Nanoimprint Lithography For High Volume HDI Manufacturing

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The growth of the electronics industry has resulted in a greater demand for high density interconnect (HDI) structures. HDI structures are used to meet the demands for lighter, more compact devices that offer superior performance. Examples of such HDIs are rigid or flexible micro-via PWBs, chip-scale package substrates and ceramics-based substrates. HDIs find applications in ink jets, automotive displays, computer hard disk drives, mobile phones, telecommunication equipment, high-end IC packaging, flat panel displays, chip on suspension and medical device applications. However, conventional electronics manufacturing technologies have processing limitations, low manufacturing yields, high production costs and limited flexibility for HDI applications. Such drawbacks have resulted in the need for alternative technologies capable of meeting market demands. Nanoimprint lithography (NIL) is a new technology which can improve cycle time, ensure yields and reduce production costs in the manufacture of flexible, rigid-flexible or HDI circuits, for example. The technology allows for the manufacturing of complex multi-layer circuits with tracks and vias with linewidths down to a few microns.

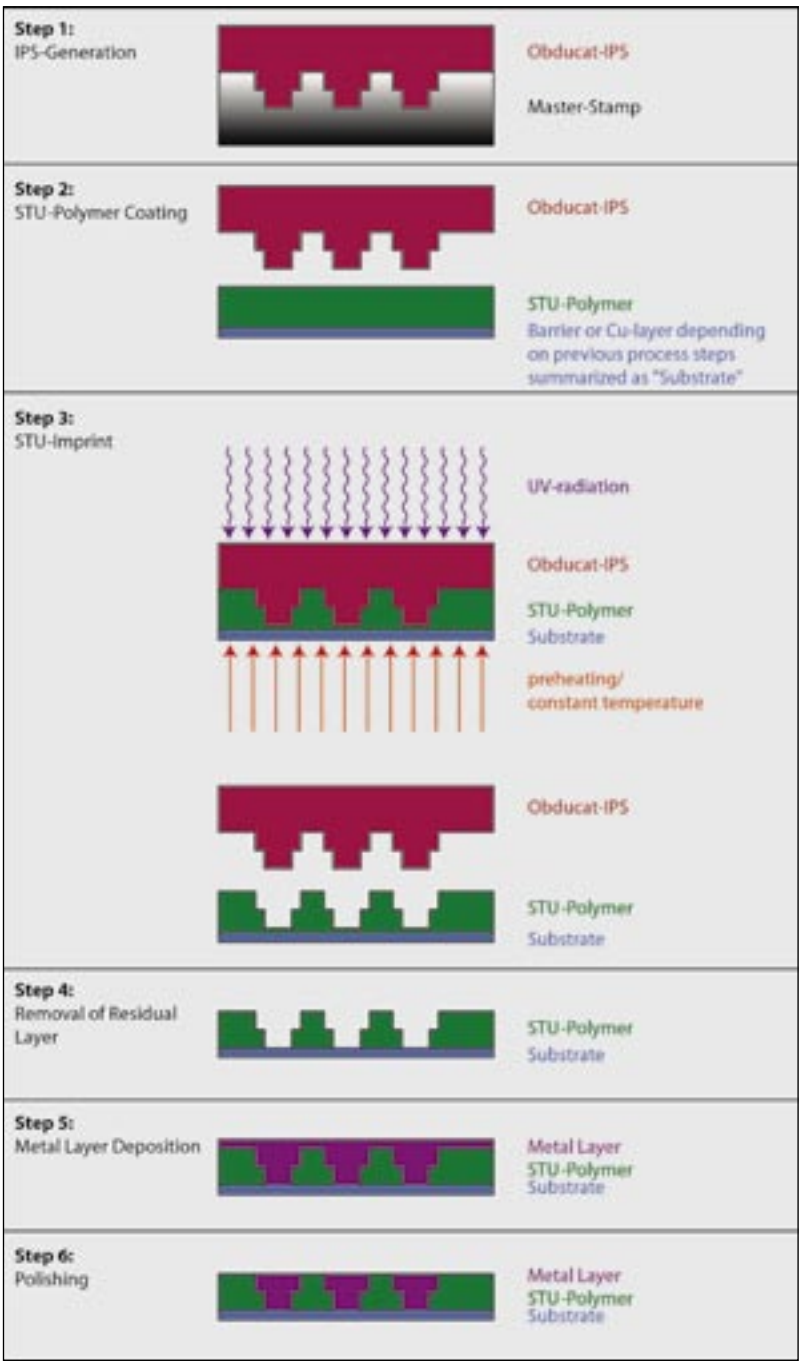


Figure 1 - Process flow for creation of an HDI double layer comprising conductive layer and vias

Some years ago, nanoimprint lithography (NIL) was considered to be one of the most promising candidates for large-scale production of nanometer-sized structures. Since then several research groups and companies around the world have spent a lot of time developing equipment and processes for a large number of applications. Global players within the semiconductor and electronics industry have been and still are evaluating NIL for their purposes. The results from these efforts prove that nanoimprint lithography is not only by far the fastest method available for nanoreplication, it also offers unbeatable resolution. Furthermore, it has also been shown that the technology offers fabrication advantages for much larger structures residing in the micrometer range, such as HDI. Today, the

first companies have started producing components using NIL.

In the following, the focus is on the imprint of HDI structures employing a three level imprint template. We take a look at the benefits arising from NIL for HDI applications and also present an alternative concept for high volume manufacturing using NIL.

UV-lithography and nanoimprint lithography: a comparison

In a traditional UV-lithography-based process for interconnects, numerous steps are required to generate one conductive layer and the via holes. The process includes steps such as resist deposition, photolithography, development, deposition of metal layers and dielectric layers, polishing, laminating, and so on.

Nanoimprint lithography is a promising technology as it enables multiple layers to be printed in a single imprint step by employing a multilayered stamp. By doing so, the imprinted polymer can serve as the dielectric layer, reducing the number of process steps significantly, down to 5-6 steps per double layer depending on the stamp material used. The three-dimensional structures obtained after imprint can finally be filled with conductive material, preferably Copper. The reduction of process steps will therefore result in a significant reduction in process costs.

The process can be performed using a hard stamp material such as Silicon, Nickel, or quartz, as well as Obducat's proprietary IPS-STU process involving polymer stamps. Soft-press NIL technology is necessary to achieve good results in terms of a homogeneously distributed residual layer thickness after imprint. Both technology and process are currently combined in a high volume manufacturing tool (Figure 2).

The IPS-STU concept

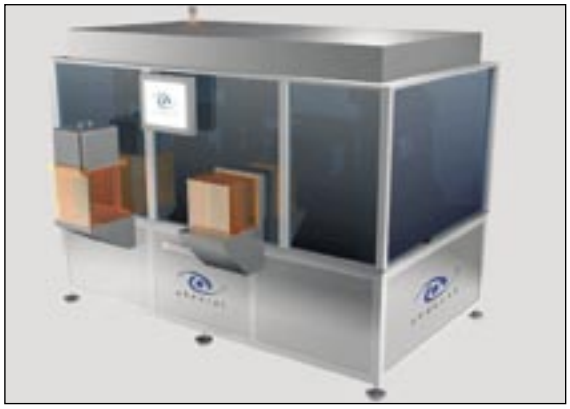
As illustrated in Figure 1, the process sequence starts with step 1 generating an intermediate polymer stamp (IPS) from a hard master stamp (Si, Ni or quartz) by an imprint process. In a second imprint (step 3 in Figure 1) the IPS is used as a single use template in a simultaneous thermal and UV-process (STU). The two imprint steps are performed in parallel at different locations inside the HVM tool to increase throughput. An illustration of the HVM tool configured for wafer scale imprinting of wafers up to 8" diameter is shown in Figure 2.

Since Obducat's soft-press technology employs compressed gas rather than rigid material, homogeneous pressure distribution across the entire imprint area can be guaranteed along with the possibility of increasing the imprint area to any desired size or shape in customer specific tools. Soft press technology thereby enables printing to take place on large substrates i.e. PCBs or glass for flat panel displays.

Further benefits of the IPS-STU-concept are reduced defect area, longer lifetime of the master stamp material, lower cost of ownership and increased cleanliness through self-cleaning of the master. A comparison between traditional NIL employing hard stamps and the IPS-STU concept employing single-use polymer replicas is illustrated in Figure 3.

A three-level master stamp can be produced easily by standard UV lithography and ICP etching. Subsequent coating with a monomolecular anti-adhesion layer enables reproduction into a large number of IPSs by imprinting. No polymer residues adhere to the master making intermediate cleaning procedures obsolete. The separation between master and IPS is performed automatically.

Figure 2 – A first generation IPS-STU HVM-tool with FOUPs for substrates up to 8 inches in diameter. The soft press technology is scalable and second generation tools that can handle larger area substrates will follow



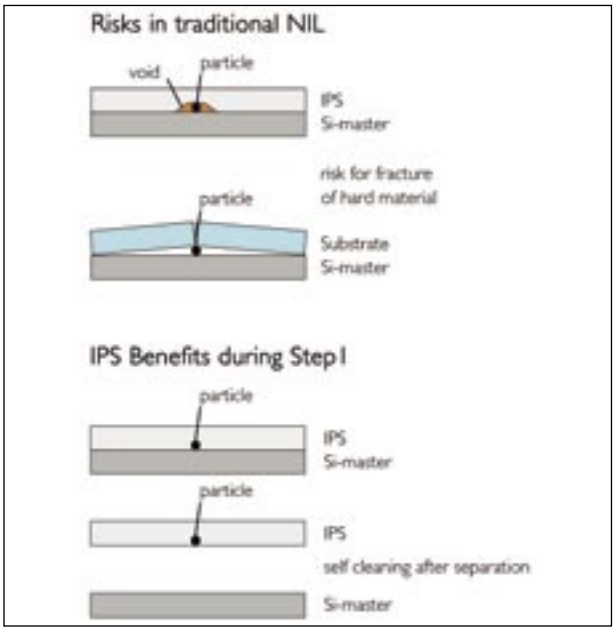


Figure 3 - Comparison between traditional hard stamp NIL and the IPS technique

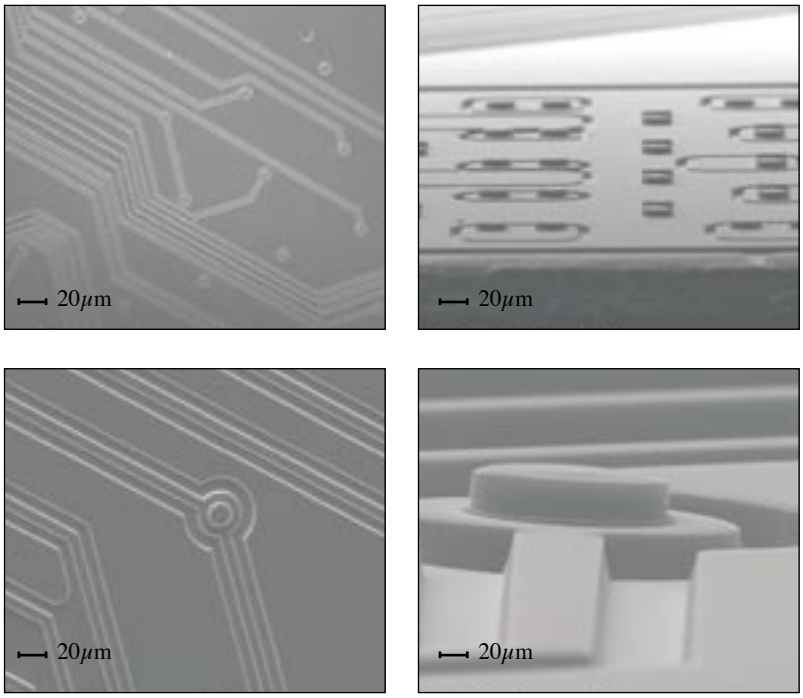


Figure 4 - SEM micrographs of an IPS with HDI pattern containing structures for via holes and connectors. The IPS was sputtered with a metal layer prior to the SEM investigation. The linewidth is 20 µm

Imprint results

Figure 4 shows SEM-images obtained after sputtering an IPS with 100nm metal. The image shows three different levels on the stamp including connectors and pillars for vias. The IPS has excellent anti-adhesion properties to the STU-polymer used during the second imprint step. Therefore it is not necessary to deposit any anti-adhesion layer on it. The STU polymer is fully compatible with the standard PCB substrate material and has similar dielectric properties, making it extremely well suited as an insulation layer for HDIs. After curing with UV light it is chemically inert, can be easily coated with more layers, and is thermally stable up to 300 degrees enabling soldering processes without degradation of the dielectric layer. This concept allows HDI PCBs to be built up layer-wise by imprinting without requiring any lamination processes.

Figure 5 shows SEM micrographs of the imprint result in STU-polymer obtained using an IPS. The imprint has been performed on a substrate spin-coated with STU-polymer. On this sample the residual layer thickness was measured to 1.4 µm, which is more than sufficient for opening up the via holes using Oxygen plasma (step 4, Figure 1). Optimisation towards thinner layers is possible if necessary and the linewidth of the structures can be reduced as well (e.g. the standard residual layer thickness for nanometer structures is below 20 nm with an accuracy of ±5 nm across a 6" wafer). The sidewall roughness is a reproduction from the master stamp and comes from the ICP etch process. The rim around the via hole is also transferred from the master, which was slightly overetched in one of the process steps. This can also be seen in one of the IPS micrographs in Figure 4. No imprint related artifacts are present in the images.

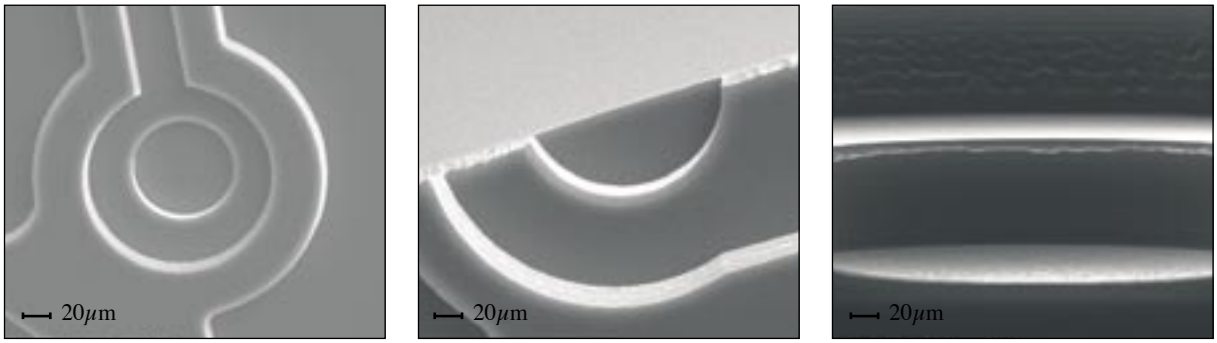
In the next step, the substrate material had to be changed from Silicon to PCB material, and imprinting with alignment to a previous layer had to be performed. The result is shown in Figure 6.

In the subsequent metal deposition step (step 5 in Figure 1) several approaches are possible, including deposition of a seed layer followed by electroplating. Other methods are under evaluation. The result is shown in the optical micrograph in Figure 7 where the dark areas correspond to metal. The cross-sectional image shows larger metal cores surrounded by the dielectric as well as via holes and interconnects on the surface of the PCB.

Nanoimprint lithography and the PCB industry

It has been shown that nanoimprint lithography has great potential to become the core production technology for advanced high density interconnects appli-

Figure 5 - SEM micrographs showing the three-level structure-imprint of an IPS. The residual layer in the vias is 1.4 µm



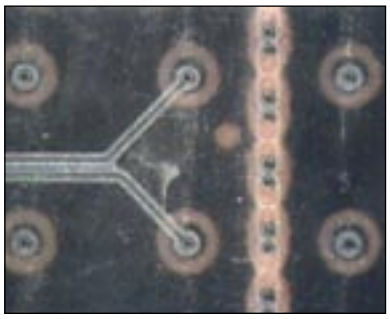
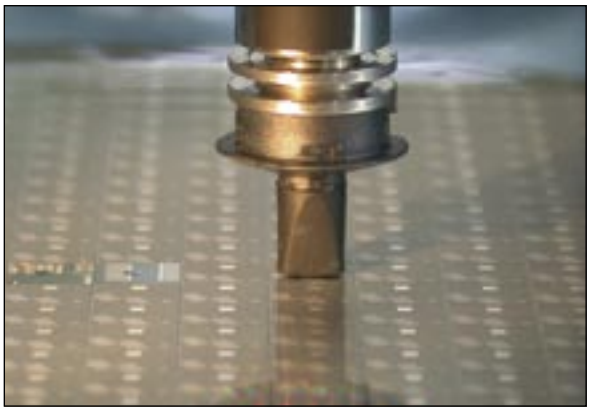


Figure 6 - Optical micrograph obtained after aligning the stamp with its via pillars and connectors to a PCB substrate with Copper pattern and printing

cations. The number of process steps reduces significantly as the imprint polymer can act as the dielectric layer itself. Soft-press technology with compressed air means that equipment can be scaled up towards the requirements of the PCB industry, thereby allowing for the printing on substrates with sizes of, for example, 18" x 24". Current development work focuses on optimisation of the alignment accuracy for the printing of entire PCB panels.

Figure 7 - Optical micrograph showing a cross-section of double side imprinted vias and traces aligned to each side of the substrate

Siplace For Die-Attach And Flip-Chip Applications



Siemens Automation and Drives (A&D) has presented its first die bonding system with the Siplace A-Series. According to Siemens, this new machine platform is ideally suited for manufacturing plants where die-attach as well as flip-chip applications must be executed with speed, flexibility and reliability. Two machine versions are available: the Siplace A1 with one gantry and the Siplace A2 with two gantries.

The Siplace A1 is a single-gantry machine featuring eutectic bonding in addition to die-attach and flip-chip bonding. The system is capable of processing more than 200 different die types and works with all types of feed systems such as wafers, waffle packs, gel packs or tapes. Passive components can also be supplied via five 8mm tape feeders. Thanks to its flexibility, the Siplace A1 is ideally suited for multi-chip applications, and with its large processing area it is capable of handling very large substrates up to 640 x 150 x 55 mm for epoxy applications and 30 x 35 mm for eutectic applications. A gantry-mounted camera ensures the high placement accuracy of up to +/– 10µm at 3 sigma and 1,500 dies per hour. The large number of stamping tools, bond tools and die ejector configurations makes the new Siplace A-Series even more flexible and functional. Like the hardware, the software is also designed for the requirements of multi-chip applications. The enhanced software package for individual die processing, features a complete range of programming options. Users can define pick-up positions and program epoxy/die placement and alignment sequences in easy steps.

The dual-gantry Siplace A2 operates with two parallel gantries. While one dispenser-equipped gantry applies the adhesive or stamps the epoxy, the second gantry places dies. Thanks to the simultaneous dispensing and bonding operations, the Siplace A2 achieves a placement performance of 3,600 dies per hour with an accuracy of +/– 12µm at 3 sigma. The substrate processing is equally flexible, because the Siplace A2 can handle boat and carrier substrates as well as strip and lead-frame substrates with sizes of up to 200 x 150 x 40 mm and die sizes ranging from 0.125 mm^2 to 25 mm^2.

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