RFID Chip Assembly For 0.1 Cents?

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While the world is arguing over the "Nickel tag," a passive RFID tag priced at 5 US cents, and whether it could be on the market by 2008, the suppliers of backend equipment are aggressively pursuing various technology avenues to decrease manufacturing costs and enable the ubiquitous use RFID tags.

The application possibilities of RFID are endless. Technical analysis shows that broad-based applications of RFID will develop in two distinct phases. Phase 1, which we are in right now, is characterised by only marginal advances because RFID is superficially tacked onto existing business processes. Phase 2 will bring about a truly revolutionary change in the global business environment, after radical process re-engineering and new RFID-centred business models emerge. This phase will unlock the full potential of RFID and turn it into a new base technology. In addition, analysts say that industry executives are focusing on the price of RFID tags and when they will come down.

Price is the significant benchmark for RFID tags to be accepted in broad-based markets. Today, there is talk of the "Nickel tag", a fully functional passive RFID transponder for just a Nickel (5 US cents) per unit. Back in 2003, the average price point of RFID tags was ten times this value. But now there is evidence of a new wave of technology enablers that will drive the production cost of RFID tags down. The focus here is the cost of chip assembly.

General technology approaches to RFID chip assembly

The method of assembling a chip onto a substrate has been developed and optimised for decades and is known as conventional die bonding technology. Based on this know-how, equipment vendors derived advanced die bonding machines which can carry out high-speed flip chip assembly. Due to the huge potential demand for RFID tags, a couple of alternative approaches (for example, Fluidic Self Assembly and Vibratory Assembly), referred to also as "visionary approaches" in this context, seem to offer solutions to the challenge (Figure 1).

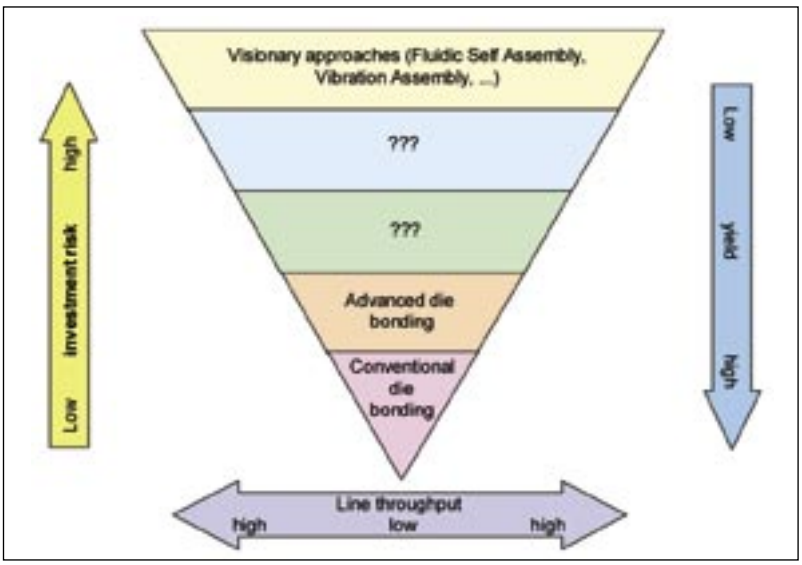


Figure 1 - Benefits and trade-offs of conventional and visionary approaches

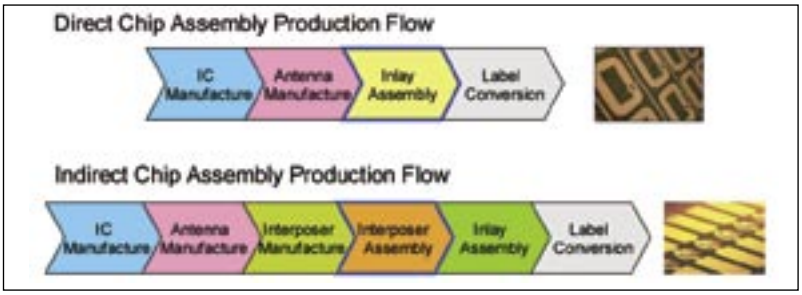


Figure 2 - Direct and indirect chip assembly production flow

The most significant advantages of conventional and advanced die bonding equipment are that they are based on mature technologies offering low investment risk and high-yield operation. To give a better idea of these advantages, consider the assembly of high-end flip chip devices like DSPs and ASICs where an assembly yield of over 99.95% is a standard target. For low-end flip chip devices like RFID tags, a yield of 98% is standard; an optimisation to 99% yield is realistic if all process and material parameters are well controlled; and 99.5% should be a reachable in the mid-term timeframe.

The following simple calculation helps explain the cost pareto of yield loss. A complete chip assembly line including adhesive application, flip chip attach, curing, testing and slitting is currently available at a market price of less than 1,000,000 US$. With 7400 hours of production time a year, a line throughput of 10000

UPH, and 5 years depreciation, the cost of chip assembly is 0.27 US cents per tag. Assume a further 15 US cents for the costs of an RFID tag and consider a yield loss of 2%. Then the cost of the yield loss is 0.3 US cents, which exceeds the depreciation costs of the equipment. This calculation should help to illustrate the high value of high-yield assembly equipment.

Direct and indirect chip assembly

In the manufacturing of RFID tags, there is a basic distinction between direct chip assembly and indirect chip assembly (Figure 2).

In direct assembly, the chip's bumps are positioned and placed directly onto the antenna connections by means of flip chip technology. The key advantage is a lower packaging cost, because this requires fewer process steps and consumes less material. However, despite the large antenna pitch, high throughput rates necessitate negligible indexing timing. Thus – with a conventional flip chip bonder approach - the technology is not without its challenges, which will be better manageable the bigger the bonding area of the antenna web. However, the trade-off with a bigger bonding area is longer travel time for chip transport. A well-balanced dimensioning of the bonding area will result in a successful machine concept (Figure 3).

As an alternative, various manufacturers employ indirect RFID chip assembly. Indirect assembly, as a first process step, introduces a flip chip interposer. In a subsequent step, at very high throughput, the interposer is mounted on the antenna, which can be done by crimping. Indirect assembly is advantageous especially for manufacturers who have no previous experience with bare-chip processing and do not want to invest in gathering the necessary know-how. At the same time, investment costs for the follow-up assembly step are significantly lower. The trade-off here is higher packaging costs. Also, crimp connection quality is still a very controversial matter. Therefore, alternative methods such as soldering or adhesive interconnection methods are being used. Or the connection is facilitated after the interposer is glued onto cardboard with the antenna being applied in a second step via the printing of conductive ink over both cardboard and interposer.

Flip chip interconnection technology and process flow

The type of interconnection method also has to be chosen. Figure 4 shows the various options that are generally available. In terms of RFID chip assembly, the most promising technologies are NCA (non-conductive adhesive) and ACA (anisotropic conductive adhesive). Since the pre-applied epoxy also functions as an underfiller, the interconnection technology is very cost-effective, especially in paste form (NCP, ACP). The epoxy can be applied by screen printing or dispensing, whereby dispensing saves further costs because the process consumes less material. Bearing in mind that NCP is less expensive than ACP, the ideal interconnection technology seems to be dispensed NCP. The advantages of NCP are: easy, fast, low-cost processing; high-quality interconnections; no additional underfill necessary; few process steps; low epoxy cost; compliancy with low-cost substrate materials; compatibility with reel-to-reel applications.

The feasibility of high-volume NCP

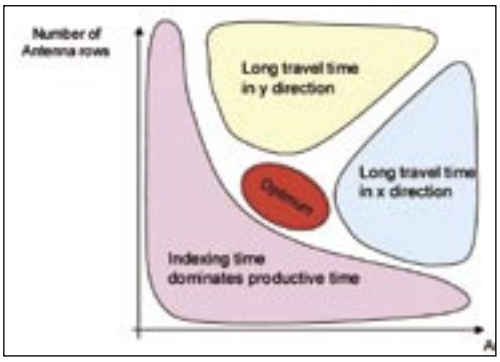


Figure 3 - Optimal machine concept requires well-balanced dimensions of the bonding area

production on flex substrate has also been demonstrated in smart card production, where the high reliability requirements of the flip-chip packages has been proven. In addition, the non-collapse soldering process is used for RFID chip assembly. For example, the GBS process (gold bump soldering) benefits from the low bumping costs of the gold bump and the high quality of the intermetallic interconnection due to soldering.

Collapse processes are not feasible because of higher bumping costs, thicker package profiles, and the

Figure 4 - General flip chip interconnection options

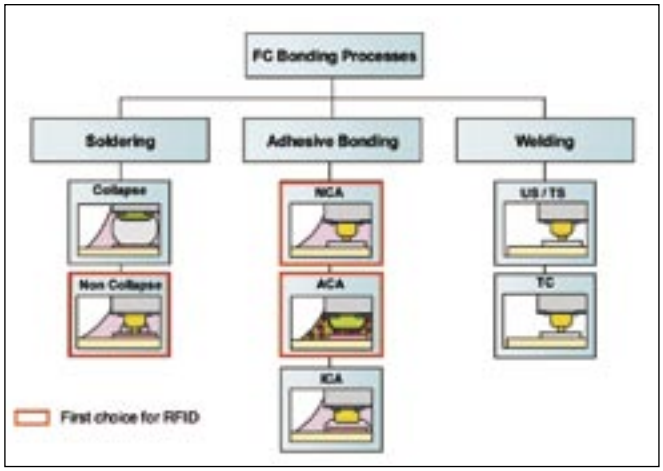
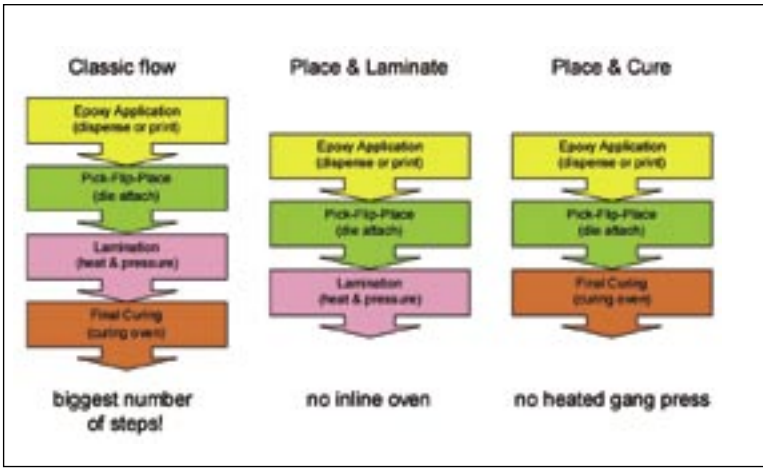


Figure 5 - Types of chip assembly process flow



IC manufacturing costs (thinned, bumped, diced wafer)	< 2 cents
Antenna manufacture	< 1 cent
Inlay assembly (including chip attach)	< 1 cent
Label conversion	< 1 cent
Total	**< 5 cents**

Table 1 – Possible cost breakdown for a 5 cent RFID tag

General assembly technology	high-speed flip chip bonding
Chip assembly method	direct chip assembly
Interconnection technology	adhesive bonding / NCP
Process flow	place & laminate
Epoxy application	dispensing
Package test	integrated
Slitting	integrated
Line throughput	10000 UPH

Table 2 - An assembly process for 4" x 1" UHF inlays

Dies per Index	Curing Dwell Time [sec]					
	2	4	6	8	10	12
4	3600	2400	1800	1400	1200	1000
6	5400	3600	2700	2200	1800	1500
8	7200	4800	3600	2900	2400	2100
12	10800	7200	5400	4300	3600	3100
16	14400	9600	7200	5800	4800	4100
20	18000	12000	9000	7200	6000	5100
24	21600	14400	10800	8600	7200	6200
36	32400	21600	16200	13000	10800	9300

Figure 6 - Throughput of a heated press for parallel lamination of dies

Depreciation costs for chip assembly	< 0.22 cents
Depreciation costs for dispensing	< 0.02 cents
Depreciation costs for test & slit	< 0.03 cents
Operating costs	< 0.06 cents
Adhesive costs	< 0.05 cents
Yield loss	< 0.3 cents
Total inlay assembly	**< 0.68 cents**

Table 3 - The cost budget per RFID tag for the inlay assembly process illustrated in Table 2

Depreciation costs for chip assembly	< 0.11 cents
Depreciation costs for dispensing	< 0.01 cents
Depreciation costs for test & slit	< 0.02 cents
Operating costs	< 0.03 cents
Adhesive costs	< 0.05 cents
Yield loss	< 0.03 cents
Total inlay assembly	**< 0.25 cents**

Table 4 – Mid-term RFID tag cost budget for the inlay assembly process illustrated in Table 2

need for an extra underfill step, unless pre-applied underfill is used. The ICA process is also inferior because it requires the extra underfilling step. Ultrasonic (US) and Thermosonic (TS) processes require a mechanically stable substrate, which is not easy to achieve with low-cost materials like PET at thicknesses of 50µ and below.

Chip assembly process flow

As a final consideration, the various options of process flow for chip assembly must be understood. The classic flow, which has been used for NCP production, starts with epoxy application (screen printing or dispensing), followed by the pick-flip-place (die attach). Curing takes place in a two-stage process: parallel lamination of a couple of dies in a heated press station (pre-curing) and final curing in an inline oven. Experience has shown that the number of process steps in the classic flow can be reduced by going with either the place and laminate flow, which does not need an inline oven for final curing, or the place and cure flow, which eliminates the lamination in the heated press.

The place and laminate flow is very widely used in RFID inlay production for NCP and ACP packages, but has its trade-offs in line throughput. Figure 6 shows the achievable throughput of a heated press as a function of the number of dies per index (to be laminated in parallel) and the curing dwell time, assuming 2 seconds for the non-productive time during index, open and close of the heated press.

Assuming 7500-10000 UPH for a flip chip bonder, depending on the antenna size, the line UPH can essentially be bottlenecked by the heated press, especially for production of big UHF inlays. This is one major reason why place and cure assembly solutions, which are standard for soldering processes, are in focus for future investments.

The 5 cent tag

Coming back to the question of whether a sales price of 5 US cents will be realistic in the next few years, a widely shared view of the RFID label's cost budget is shown in Table 1.

According to semiconductor manufacturers, RFID IC manufacturing for less than 2 cents will be realistic for high volumes. Also antenna manufacture and label conversion technologies are developing toward a cost target of less than 1 cent each. It is beyond the scope of this article to give a detailed picture of the cost map for all combinations of technological approaches for inlay assembly. Instead the cost budget for a particular turnkey assembly solution is presented, which will definitely be a benchmark for all winning technologies in the future (Tables 2 and 3).

The depreciation costs are based on 5 years and 7400 productive hours per year; operating costs are based on 30$/h including environmental costs, where each operator can serve 5 lines. Yield loss is based on 98% yield and 15 cents inlay costs.

Based on a 2-year-outlook, the author proposes that equipment suppliers will be able to double the UPH of the assembly lines at constant equipment costs, and the yield should be increased to 99.5% with inlay costs dropping below 5 cents. This results in the mid-term cost budget benchmark for RFID inlay assembly shown in Table 4.

Smart Labels, Tickets And Luggage Tags On One Machine

Melzer offers Smart Label/Smart Ticket (SL/ST) production line for smart labels, smart tickets and smart luggage tags; laminated contactless cards; eGovernment products (inlays for ePassport holder pages or eNID cards); and smart cards and dual interface cards. Among the features of the machine is the ability to automatically sort out rejects in the transponder reel fully automatically at the highest speed possible. No need for expensive pre-selected transponders or time, space and labour demanding pre-selection processes. Within a fraction of a second the SL/ST can replace a defective RFID transponder before it is attached to the product. The machines also guarantee the highest production throughput with standard transponder material. 1% rejects in the transponder reel reduce the output of the machine by less than 1%. From the extremely versatile and fast single-track version to the high-capacity four-track version, Melzer caters for every volume requirement (10,000 to 40,000 pph or max. 65 m/min to 260 m/min respectively).

Melzer, which celebrates its 50-year anniversary in 2006, is also specialised in machinery for inlays based on wire embedding technology. The company provides customised solutions when standard machines do not fit the needs of the customer.

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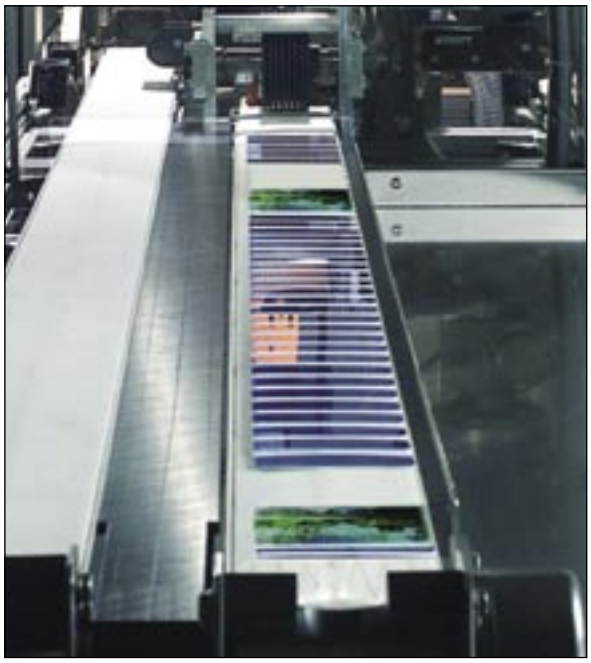
Batch Counting Option Added To Automatic Card Inspection System



Spartanics announces that a Batch Counting Option has been added to their 930 Plastic Card Inspection System, which enables users to automatically batch approved and/or reject cards into groups of a selected pre-set size. The M930 is a smart self-learning system that trains on the desired card image in minutes and totally bypasses limitations in operator training. It is a 100% reliable system according to the company and fully inspects both sides of cards at a rate of 36,000 cards/hour. The Batch Counting Option will make continuous operation of the system possible, without delays for packaging finished and inspected cards, and is available with all new systems and as a retrofit add-on.

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