A range of integrated and embedded passive component technology options are available and a number of technological and commercial barriers exist that are gating the development and uptake of this exciting new technology. In the following, we take a look at these technology options and barriers and make recommendations for building the embedded passives infrastructure.

Discrete Surface Mount passive components make up over 90 per cent of the total component count on a typical PCB today. These components also account for some 30 per cent of all solder joints and occupy close to 40 per cent of the total board area. These discrete passive components can prove even more significant in cell phone boards where up to 95 percent of the total component count, 80 per cent of the board area and 70 per cent of the board assembly costs may be attributed to the passive components.

The development of a range of integrated and embedded passive component technologies over the past decade has promised major benefits over the traditional Surface Mount discrete passive components. These include improved product performance, reduced size and weight, higher functional density, reduced mounted component numbers, reduced wiring demand at the next interconnection level, improved reliability through a reduction in solder joint count, improved EMC performance and improved design accuracy through the availability of quasi-continuous component values. Most importantly it has also been demonstrated that these performance benefits may be obtained together with a real and useful reduction in the overall product cost per function.

**Embedded passive component technology options**

Passive components integration or embedding needs to be conducted in the context of the ever-evolving packaging hierarchy. This includes the chip level (zero-level), the package level (1st level) and the PCB level (2nd level). Within this hierarchy the passive components may be incorporated as on-chip components, as Integrated Passive Device (IPD) arrays and networks, within the package level (so called System-in-Package (SiP)) and within the PCB substrate itself. Again a number of substrate technology options are available at the IPD and SiP package level, including thin film, Low Temperature Co-fired Ceramic (LTCC) and laminate based technologies.

Resistor, capacitor and inductor components may be implemented in standard Silicon integrated circuit technologies but component performance is constrained by the materials available in the Silicon technology. Inductor quality factors in particular are limited to values of below 10 by the 1 to 2µm Aluminium alloy or Copper metallisation thickness and by substrate losses in the underlying semiconducting Silicon substrate.

Work is now in hand to develop CMOS, BiCMOS, SoI and SiGe processes with improved passive component performance. These new processes employ thick Copper metallisations, polysilicon ground shields and thick redistribution dielectric layers that together can achieve inductor quality factors of up to 30. Dedicated integrated capacitor layers are being introduced for higher capacitance density together with resistor layers that provide improved accuracy and...
lower temperature coefficient of resistance.

Passive inductor and capacitor components are less amenable to scaling than active IC components and so the use of such on-chip passive components adds a chip area (and associated cost) overhead of up to 0.5mm² per component. On-chip passives are therefore best employed in circuits where a few, performance critical components are required, for example in Voltage Controlled Oscillators (VCOs) (Figure 1).

The closely related integrated passive thin film technology category employs Silicon-like processing technology to provide precision passive component arrays, networks, IPDs and substrates for high functional density SiP applications. High resistivity Silicon wafers, glass wafers or large area panel substrates are employed for the thin film manufacturing process. A sequence of metal and dielectric layers are deposited by a combination of sputter deposition, electroplating, anodisation, chemical vapour deposition and spin coating and patterned by photolithography and wet and dry etching techniques in typically 5 to 8 masking operations. Conductor and interlayer dielectric layers are in the 2 to 10µm thickness range.

The Thin Film approach

The thin film resistor materials include nichrome and tantalum nitride for low TCR resistor components at 25 to 100 ohms/square. The capacitor and interlayer dielectric layers include anodised aluminium oxide or tantalum pentoxide, silicon nitride and benzocyclobutene (BCB) or polyimide materials to realise capacitor components with capacitance densities between 4pF and 1,000pF/mm². The conductor materials that provide the passive component electrodes, the ground plane, inductor elements, controlled impedance interconnection traces and active component and next level interconnection pads include Aluminium and Copper with the addition of Nickel-Gold surface finish layers where required for wire bondability and solderability.

The thin film technology option provides a full range of precision passive components (Figure 2) with inductor quality factors of up to 70 through the use of low loss substrate materials. This technology option is well suited for high-density passives applications (over 100 passives/cm²) in the realisation of small matching and filtering networks (a few mm²) and for networks, arrays and SiP substrates up to 1cm² in area. The technology has the advantage of compatibility with active device technology and the emerging MEMS technologies and is manufactured today by a number of IC companies to leverage and add value to their Silicon IC product offerings.

The Low Temperature Co-fired Ceramic approach

The LTCC integrated passives technology options has its origins in thick film hybrid technology using screen printed and fired thick film materials. The LTCC material itself comprises an unfired (so called “green”) glass-ceramic material held together with a polymeric binder. Interlayer vias are drilled or punched and metallised and thick film conductor, resistor and dielectric patterns are printed onto the green LTCC layers. Multiple LTCC layers are then laminated and fired to produce a fully dense multilayer substrate structure with integrated passive components and interconnection structures. Additional surface layer components may then be printed and fired and accessible components laser trimmed as required. Lithographic patterning and zero-in-plane-shrinkage technologies have been introduced in recent years to increase pattern accuracy to below 25µm feature size and to improve dimensional control.

A wide range of thick film resistor, dielectric and conductor materials is available. Resistor materials cover the range from 10 ohms/square to 1 Mohm/square, although buried resistor layers are best limited to a narrower range. Paraelectric and ferroelectric dielectric materials are available with dielectric constants from 5 to in excess of 2,000 at a typical minimum layer thickness of 10µm. Silver and silver alloy conductor layers are widely employed in LTCC technology with a typical layer thickness of 10 to 15µm. This substantial metal thickness leads to high inductor quality factors at ~1GHz frequencies.

The LTCC technology offers a cost effective, rigid, stable and repeatable substrate medium that includes a wide range of passive component elements, with the option of component trimming for circuit tuning. The LTCC medium also provides a built-in active and discrete passive device packaging and interconnec-
tation structure. This technology option has been adopted for the volume manufacture of a range of RF SiP modules for applications such as the Bluetooth RF front-end and related transceiver functions with substrate areas of up to 2cm² (Figure 3).

The Laminate Embedded Passives approach

The last category of integrated passive component technologies is the printed circuit board or laminate embedded passives category. Here the additional materials required are built into the original laminate layers that are subsequently bonded together and processed to form the multilayer circuit board structure. This is done in such a way that relatively minor modifications to established PCB processes are required. This technology is employed for the realisation of board level passive integration and in the manufacture of larger area SiP substrates (up to 25cm²). Embedded passive component densities of up to 5 passives per cm² are typical in today’s technology.

PCB embedded resistor components are realised using ~100nm electroless Nickel-Phosphorus deposits, sputter deposited nichrome or chemical combustion deposited platinum alloy layers. Resistivity levels of 50 to 1,000 ohms/square are achieved. Polymer thick film resistor materials at over 10µm thickness and covering a much wider range of resistivity values are also available. Embedded capacitor technology options include distributed planar capacitor technologies to provide board level decoupling and discrete capacitor technologies. The former category is the most advanced and employs unfilled and ferroelectric filled polymer dielectric layers at above 10µm thickness. Thin film paraelectric and ferroelectric technologies have also been developed. Inductor components can use the PCB metallisation structures already available within the board technology, although due attention must be given to component design and to ground plane and routing keep-outs. A very interesting PCB embedded passives technology class has also been developed based around the co-firing of thick film materials onto Copper foil prior to laminate manufacture.

The PCB embedded technology offers a large area manufacturing, low cost per unit area technology option that is well suited to board level and SiP passive component integration. A range of materials and technology options are available from a number of PCB materials vendors. Embedded resistor technologies and distributed capacitor technologies are finding first applications for board level termination and pull-up resistor functions and for board level decoupling (Figure 4). Discrete capacitor and inductor applications are presently less well developed.

Technology barriers and infrastructure requirements

Discrete Surface Mount passive components are provided in a limited number of standardised component form factors (0603, 0402, 0201 etc) and this makes it possible to quickly change passive component values and realise simple design iterations during New Product Introduction (NPI) without requiring changes in the board design and layout. The adoption of any of various classes of integrated or embedded passive component technology on the other hand precludes changing component values without making mask changes and completing further substrate or panel processing runs since the components, by definition, are contained within the substrate structure. This can result in increased design iteration cycle time and drives the need for a “right-first-time” design approach for integrated passives technologies, together with an NPI strategy than minimises the need for design iterations.

A “right-first-time” design approach can be achieved through the development of a technology specific “design-kit” that includes the full range of passive and interconnection and assembly component symbols...
that will be used during circuit schematic capture and simulation. Each component symbol contains the appropriate equivalent circuit electrical model, and may be linked into component physical layout generation. The generation of such a design-kit requires a well-defined process architecture with a stable manufacturing process that has known or at least tightly specified process capabilities. Technology characterisation substrates or panels have to be produced that include the full range of passive component families and inter-connection and assembly components that span the full range of component geometries within each family. Electrical measurements are followed by equivalent circuit model generation and the construction of the design-kit.

This design approach has been ably demonstrated in the thin film technology option outlined earlier in this paper. Of particular note has been the generation of scalable, parameterised, lumped element equivalent circuit models in which the primary component value and all the component parasitics are expressed as a function of a single parameter, for example the capacitor dimension or the number of turns in the inductor. This in turn allows straightforward design optimisation. An example lumped element equivalent circuit model for a thin film inductor and the close agreement of the measured and modelled s-parameters are illustrated in Figure 5.

A typical design flow then includes design specification, schematic capture, simulation and optimisation, component generation and layout, re-simulation as required followed by design-for-test, design tolerance analysis and yield modelling (Figure 6). The inclusion of individual circuit functional blocks and design variants in the NPI substrate or panel layout also minimises the need for design iterations. An example of a thin film integrated passives filter design that shows very close agreement between the circuit simulation and measured results from the first substrate processing run is illustrated in Figure 7. A more complex SiP module example containing a range of integrated passive circuit elements for matching, filtering, biasing and interconnection functions and a number of Silicon and gallium arsenide active devices is illustrated in Figure 8.

The integrated passives industry will need to put in place a set of design-kits for each specific technology definition and architecture variant in a similar way that each Silicon integrated circuit process today has it’s own process specific models and design kits. The demonstration of compatible and common form-fit-and-function will also be required from multiple suppliers so that end-users have more than one single source of technology supply. This requirement has already been demonstrated and met for both thin film and for LTCC technology implementations from different sources.

Conclusions

A wide range of integrated and embedded passive component technology options are available that promise a range of performance and costs benefits across the packaging hierarchy. The development of technology specific design-kits provides a route to right-first-time design and removes one key barrier to the successful commercial exploitation of this exciting new technology. The establishment of design and supply chain partnerships will play an important part in the establishment of the integrated and embedded passives infrastructure.