

Design For Testability – The Importance Of Simple Solutions

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While PCB component complexity and density continues to increase, making it easier to create defects and more difficult to find them, quality requirements remain the same: faulty assemblies must not be delivered to clients. In this scenario, we take a look at the evolution of test methodologies and the best approaches for the assembled boards of the future.

Since the early days of electronic components, failures have continuously existed. Despite the enormous improvements in development and production, this situation has not changed. Even automated manufacturing equipment continues to create faults on circuit boards. There is not a single PCB manufacturing technique that is 100 percent fault-free. Every new technology creates new challenges and calls for new test methodologies to ensure fault free boards. The increasing density and complexity of components is a critical factor among the causes of faults. However, the requirements remain the same: faulty assemblies must not be delivered to clients and so the need for testing remains the same.

Today, there are several test tech-

nologies available – In-Circuit-Test (ICT), Flying Probe Test (FPT), Functional Test (FT), Automated Optical Inspection (AOI) and Boundary Scan Test – each with its pros and cons. However, there is one factor that is going to be more and more decisive: costs. The costs of each test technology depend on the purchase costs and, in addition, to the costs to implement the test process, including test preparation, test execution and failure search.

Decisions on which test technology to use should not be based exclusively on costs. Analysing the specifications is important as each has its own unique implementation issues.

Disadvantages of various test techniques

The disadvantages each of the test techniques mentioned above are listed below.

Functional Test has intensive test program creation costs as well as high costs associated with troubleshooting when a fault occurs as it must be executed by well-trained personnel. Moreover, the testing of all functions and obtaining 100 percent coverage is practically impossible.

In-Circuit-Test features high costs for developing and preparing test object specific test-fixtures, extra costs if a layout change is required and very high costs for storage and maintenance of the adapters. Furthermore, probe (nail) placement becomes more and more difficult with increasing density of circuit board traces. Access to high lead count BGAs via nails is nearly impossible; it makes no sense to contact the pads because the advantage of very large-scale integration (VLSI) – namely the space saving – would be lost.

Automated Optical Inspection cannot detect faults underneath components and electric faults likewise cannot be detected.

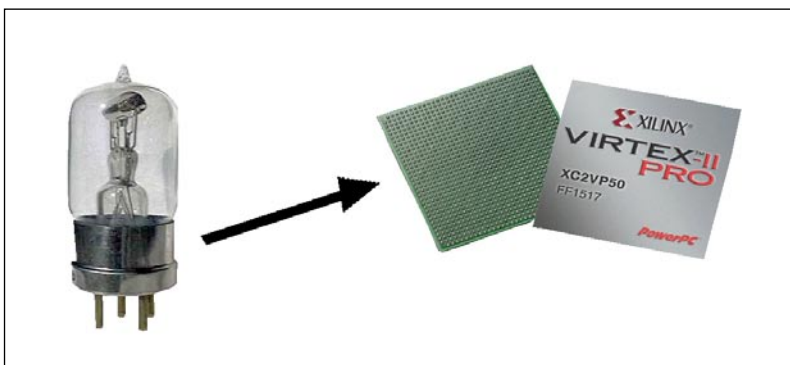
Finally, Flying Probe Test is time consuming because of the sequential contacting of the test points and the technique also features maintenance costs for worn contact pins and moved mechanical components.

“Test friendly” design of digital circuits

It may be possible to limit the drawbacks of the test technologies mentioned above by taking advantage of the features of the components of the circuits. The basic requirement is the development of a test concept with all required hardware and software elements in the unit to be tested. This endeavour is known as “test-oriented layout” or more commonly named “Design for Testability (DFT)”.

If objects to be tested are investigated, one notices that the use of digital circuits have increased in the last few years. One example can be found in the modern

Figure 1 – The complexity and density of components for PCB has continuously increased over the years



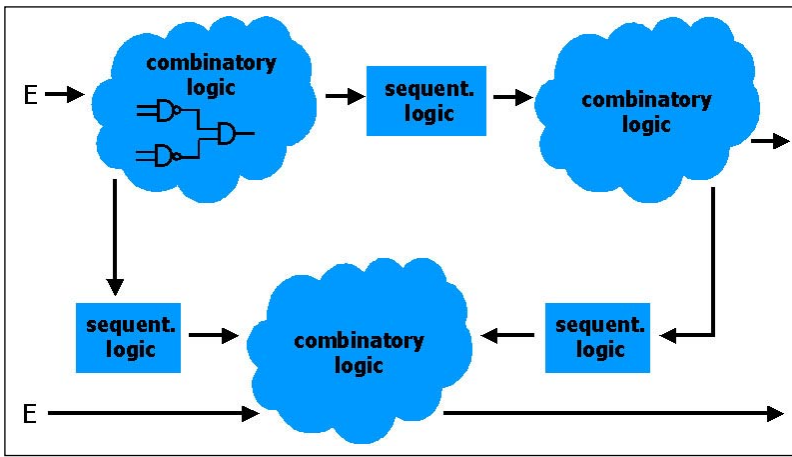


Figure 2 – Parts of a digital circuit

consumer electronics. The trend from analogue to digital technology is clear, especially in the case of radios and TVs. This trend must be considered when choosing the right test strategy, as problems in testing digital circuits play a decisive role. There are two major issues with the examination of digital circuits: test pattern generation and test verification.

Test pattern generation is the process of producing stimulus signals for a circuit, in order to prove its correct functioning.

Test verification is the determination of the response of the circuit.

Both automatic test pattern generation and test verification have been becoming more and more difficult due to increasing board complexity. This can best be clarified by considering a functional test as example. Therefore it is assumed that each digital circuit can be broken down into sequential and combinatorial circuit parts.

According to Moore and McCluskey, the minimum number of test vectors, Q , for 100% functional testing (in other words: how many test vectors are necessary to test all possible functions of a circuit) is calculated with the formula:

$$Q = 2^{(x+y)}$$

Where x is number of inputs and y is number of storage elements (sequential circuit parts).

For a hypothetical circuit with 25 inputs (x) and 50 internal latches (y), a test rate of 100ns per test step requires a test time of 10^7 years.

This testing problem can be avoided by designing circuits which are more efficiently testable – using the sequential circuit parts. That means that the circuit must be designed to be testable up to an

acceptable fault coverage in an acceptable amount of time and, furthermore, to overcome the problem of test access. This “test friendly” layout is called Design for Testability. Design for Testability is divided into two groups: Ad-Hoc-Design and Structured Design.

Ad hoc design

Ad-Hoc-Design consists in the creation of partitions in the circuit, the importing of additional test points and the use of bus architectures. Partitioning means the breakdown of the circuit into smaller parts which are easier to test. The sum of the effort to test each of these parts is considerably less compared to the effort in testing the entire circuit. Bus architectures simplify the testability by selectively activating the individual bus participants.

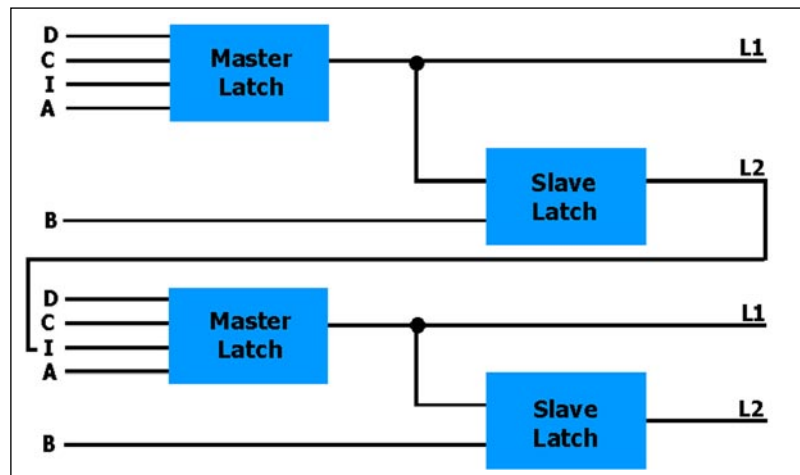
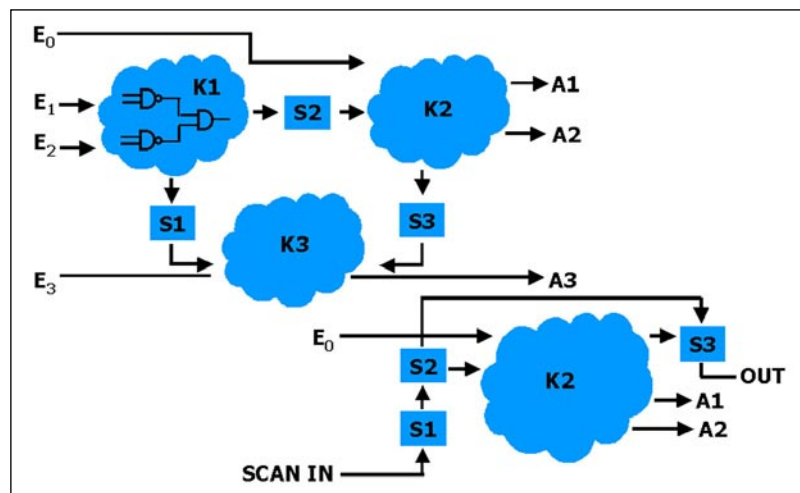


Figure 3 – Block diagram LSSD

Figure 4 – Sequential logic as “tester”



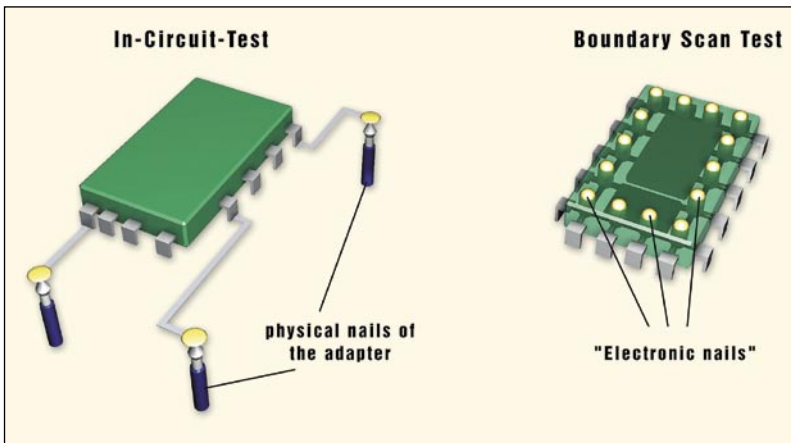


Figure 5 – Principle of the ICT compared to the Boundary Scan test

Structured design

Structured Design's aim is to reduce the sequential complexity of a network in order to simplify the test pattern generation and test verification. This aim is achieved by creating possibilities to control and observe the state of sequential machines. Methods that implement these two types of circuitry are called "passive test aids".

One of these passive test aids, which has become accepted as a systematic aid and in the meantime has become a standard for the manufacturers of mainframe computers is the Scan Path method. Using this method, circuits with sequential storage elements can be subdivided into observable and controllable combinatorial circuit parts. Therefore, the storage elements' internal states are required to be controllable and observable. This can be achieved by interconnecting the internal storage elements to shift registers, in order

to enable the serial insertion of test items and the serial read-out of test answers. The classic Scan Path method is the LSSD (Level Sensitive Scan Design), which was developed by IBM for mainframe computers in the 1960s. It is based on the extension of functional storage elements to shift register elements, the so called "shift register latches" (SRL).

In normal operations the SRL works as latch ($A=B=0$) with data input D, clock input C and data output L1. In the test mode it takes the function of a shift register cell ($C=0$). The shift data input I is connected with the shift data output L2 of the previous cell. The data are switched from L2 to the I of the next cell. The clock inputs A/Master Clock and B/Slave Clock are set in alternating fashion and cause the shift process.

The LSSD example shows how the Scan Path Method breaks down complex sequential circuits into

manageable, purely combinatorial circuits. Since combinatorial circuits, in contrast to sequential circuits, are testable with substantially fewer test vectors, test expenditure and testing times are significantly less.

Figure 4 indicates that the example circuit breaks down into combinatorial blocks, which are tested partly by the external lines, but also – and this is important – by the internal sequential logic. The disadvantage of the sequential logic is changed into the advantage of its employment as part of the test machinery.

Application to PCBs

It seems logical that the described DFT methods, which have their roots in circuit technology, also apply to PCBs. If the technology is applicable for circuits it must be transformed to assemblies. What is needed?

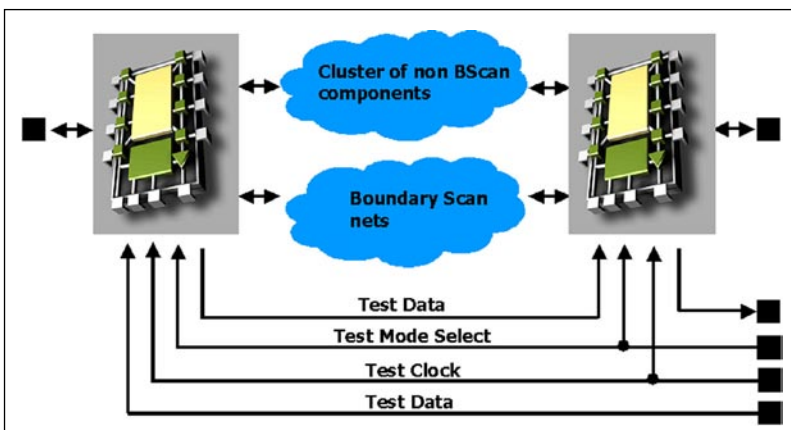
Test cells are required between the circuits. The test cells must be switchable as shift chains as well as controllable and readable via few lines. If these test points are placed in the lines they are used for In-Circuit Test. But the increasing complexity of today's boards demands the integration of these test points in the components to clear additional space for nets.

This "test friendly" requirement is ideally met by Boundary Scan, also known as JTAG. Boundary Scan has evolved to a standardised test of components and their interconnection networks.

Boundary Scan – principle and employment

Boundary Scan is possibly the most resourceful test technique which – in a similar way to the In-Circuit Test (ICT) but without physical contact – detects the failure location, sets thousands of test points (if necessary also under

Figure 6 – Principle of the JTAG/TBoundary Scan test



BGAs) and needs only four lines. While ICT is only possible with specially constructed adapters, a Boundary Scan test is already useful if there is at least one Boundary Scan component on the board.

Boundary Scan essentially means "testing at the periphery (boundary)" of an IC. Besides the core logic and the contact points some additional logic is implemented in an IC. These test points are integrated between the core logic and the physical pins. Figure 5 illustrates this graphically as compared to the principle of ICT.

Boundary Scan is simply and universally adaptable. In general one can argue that the technology supports the product throughout its entire life cycle. Already on the design stage, tests are possible by means of the CAD data, which also can be used later – even up to the customer's application. That means that test pattern created for design verification can be reused for prototype debugging and fabrication tests.

This is an important advantage since especially during the design of highly complex assemblies, their

testability for the future has to be considered.

Thus, the time and effort required for testing is enormously reduced. Only a few days or even hours are required to generate test programmes – compared with the extensive efforts required by In-Circuit or Functional Tests. Furthermore, diagnosis times are minimised, not to mention the high production costs of nail bed adapters (some tens of thousands of US dollars). Tremendous capacities and long storage times for these adapters can also be avoided.

Solution For High Volume Production Of 3D MIDs

A new LpKF laser system increases the throughput of three dimensional circuit carriers (3D-MIDs) enabling the solution to be used for volume production. Up to four laser scanners structure the components simultaneously from different angles. Machining the component in this way eliminates nonproductive times caused by workpiece repositioning. The working area accommodates two components to reduce idle time further during fully automatic workpiece loading and unloading.



tions, and who will also benefit from tool-less production. TRW Automotive, for example, builds more functions into car steering wheels using MIDs. By eliminating connectors, PCBs and cable harnesses it frees up space for new functions while saving assembly costs at the same time.

The system targets mainly the telecommunication and automotive technology manufacturers, who require fast and inexpensive mass-production solu-

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RFID Antennas For Automotive Passive Entry Applications



Premo presents a new antenna for applications in low frequency (125KHz) base stations specifically designed for those applications in which it is necessary to get a long read range with a minimum size on the PCB. The antenna has dimensions 76mm x 16mm x 5.5mm. According to the manufacturer, it is well-suited for use in vehicle passive entry applications or TPMS (Tyre Pressure Monitoring systems). The complement to this transmitter antenna are the Premo

RFID receiver antenna 3DC1111LP in base stations implemented with ATA5278 chips (base station) and with receiver elements that support 3D functionality implemented with the ATA5282.

The inductance of new antenna ranges between 200 microhenry up to 1 millihenry with quality factors between 80 and 150.

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