Designers developing today’s complex PCBs containing advanced busses sharing various voltage ranges suffer time consuming and costly power integrity problems. Traditional methods of designing complex PCBs and their power distribution systems (PDS) in particular, cost companies’ time and money at both the design and manufacturing stages. In the following, a new approach to power integrity that reduces the number of layers required in a board and eliminates panic approaches such as adding ‘fear capacitors’ or extra board layers is proposed. The core concept behind this concurrent analysis approach involves designing the PDS first to guarantee positive power integrity results from the earliest stage possible.

Overall board power integrity, EMC and the power supply system

The overall performance and EMC behaviour of electronic equipment is not only determined by the design of the circuitry and geometry of the layout, but also by the power distribution system. Parasitic noise voltages on the power/ground system caused by the fast switching of currents from integrated circuits (ICs) can lead to malfunctions and significant increases in electromagnetic emissions. High-speed components that utilise numerous complex high-pinout ICs, like FPGAs and CPUs operating on multiple voltage rails, add fuel to the fire. As these ICs become more of a commodity in electronics applications, the fight for the board space required to successfully transmit signals gets more aggressive. The smallest change in component selection, placement, routing or power/ground plane design can have a dramatic impact on the overall system performance.

The PDS is just as critical. With the job of providing operational voltage, supplying the current demands of all the active circuits, providing reference levels, implementing the current return paths for all the signal loops and compensating for external noise, power distribution needs to be designed rather than created by simply flooding layers with copper. Other technology issues that reinforce the need to design rather than simply create, include the need to provide charge over a wide frequency range, from low (e.g., system peripherals like disk drives) up to high frequencies getting into the GHz range. The ongoing lowering of supply voltages and noise margins of today’s ICs make the design of the PDS and definition of its target impedances a major design challenge.

Designing the PDS right-first-time

Back when designers only had to deal with a few voltages, there was little need for extensive design to create a power distribution system. The overall board design process would start with the placement of ICs and routing of regular traces, followed finally by a definition of the area allocated for the PDS. The final stage in this process was simply to connect all the ICs to the PDS. The increased complexity and density of boards means that this simple approach is not as effective as it once was. The final stage is no longer just about connecting from A to B; purely because it is no longer physically possible.

With today’s complex boards the approach has been to incorporate different layers for different voltages - this has a knock-on negative impact on the cost of both design and manufacture. Alternatively, extra
‘fear capacitors’ can be placed on a board in the final stages of design to achieve power integrity. Again, this increases cost in both additional components and manufacturing. The recommended option that eliminates the requirement of extra layers or ‘fear capacitors’, involves designing the PDS first and then placing the other components around this – ensuring power integrity from stage one.

Effective PDS design

Fast analysis methodology including what-if capabilities for concurrent power integrity analysis is required. Full wave 3D solutions, that can provide highly accurate results, unfortunately are not applicable within the design process of most electronic systems where time to market and time to volume are key. A systematic approach that provides design arbitration to achieve a balance between conflicting constraints is essential. The concept is simple: optimise analysis time invested to achieve reliable decision making results. In order to accomplish this, the new methodology requires that the available data is utilised throughout the design process and that design consistency is maintained at all levels. EDA tools must manage the various design constraints with the ability to arbitrate between conflicting requirements.

A concurrent design solution, such as Zuken’s CR-5000 Lightning, integrates the power integrity methodology into the layout phase of the design process and ensures that a consistent set of design constraints, including the power distribution and de-coupling requirements, is maintained throughout the design flow. Integrated EMC and power integrity verification is available within CR-5000 Lightning; where constraints conflict, this approach enables them to be resolved early in the design process.

As an example, consider a car navigation system that includes a very small board with a fixed form factor. The unit needs to fit into the radio slot within the car. Boards like these feature high density IC technology such as FPGAs and CPUs, all with fast DDR2 memories and high-speed data links. The board also has to conform to a set power supply environment defined by the car manufacturer, and must comply to very strict EMC limits. The challenge is then to fulfil all these demands to ensure power and signal integrity and guarantee EMC. The PDS is designed first and all the components are then placed and routed using the initial PDS design.

Just as signal integrity for high-speed systems requires us to organise the topology of connections to achieve clean signals, the topology of power distribution systems must now be deliberately designed to prevent power integrity problems. Only by careful design using concurrent analysis can costly extra board layers and increased component and manufacturing costs be avoided.