BGA Breakout Challenges

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The routing of large pin-count and dense BGAs has a significant impact on the cost of the PCB, primarily in terms of layer count and via technology. Considerable research has been done with the intent of providing a general flow solution to the BGA breakout problem. The results indicate the need for collaboration between chip, package and PCB designers - emphasising the dependencies that need to be managed to reduce board costs.

The number of variables confronted in large BGA routing is significant. We take a look at solutions based on a logical analysis of ASIC and FPGA BGA pin density, array patterns, packaging requirements, pin swap constraints, layers, via technology, topology planning and routing methods.

Using a BGA is the most common method today for packaging a high pin-count or very dense ASICs and FPGAs. BGAs have been proven to be a reliable, cost effective package while at the same time providing flexibility to address miniaturisation and functional requirements. However, the increasing pin-count and decreasing pin-pitch creates a significant problem for PCB designers who must minimise layer count (to reduce fabrication costs) and fulfil signal integrity requirements (to meet the high performance goals). Most PCB designers who are using leading edge BGAs claim that the breakout of the device is the greatest contributor to the number of PCB layers. The term “BGA breakout” means applying a fanout solution and routing traces from those fanouts to the perimeter of the device prior to general routing of the PCB. Low pin-count devices (less than 500 pins), even with a pin-pitch of less than 0.8mm, do not present a significant breakout problem and are usually routed without a “breakout” method.

The BGA breakout challenge starts with over 1000 pins and 1mm pin-pitch. The largest FPGA in production today is the Xilinx Virtex-4 and Virtex-5 FF1760 series with 1760 pins and a 1mm pin-pitch. The future will bring over 2000 pins and a 0.8mm pin-pitch.

During the past year, a team at Mentor Graphics researched the existing methods for routing large BGAs with the intent of finding both interactive and automatic routing solutions for the short-term and long-term. The methods presented below address the 1760
pin / 1mm pitch devices well and touch upon methods for the future devices.

**Reality strikes**

Initial research on the subject of BGA breakouts took the team into the realm of theoretical solutions. It wasn’t long before it became apparent that most of the theory in this area breaks down when confronted with the reality of attaining reasonable manufacturing costs and fulfilling the signal integrity requirements.

There are numerous papers offering mathematical solutions to high pin-count devices in which the minimum number of layers can be calculated and various patterns for the traces are shown. Unfortunately, these proposals do not account for the impact of power and ground pins, the distribution FPGA banks in various arrangements (with the requirement that all signals in the bank need to have the same reference plane), reasonable design rules to reduce crosstalk, and nets that should be routed as differential pairs - or worse yet, nets that can be routed either as single-ended or differential pairs depending on the performance goals of the circuit.

Along with mathematical solutions, there are a plethora of proposals for spacing and aligning fanout vias. While it is true that the fanout method is the key to a successful breakout; it is not true that any one method can be applied to all situations especially when the stackup and via models are usually chosen on a fabrication cost basis.

**Compromise**

The art of engineering is to appropriately compromise the myriad of variables and still have the project fulfill the time, cost and performance goals. In the context of BGA breakouts, there are indeed a myriad of variables; however, these are the ones that have the greatest impact on cost and performance:

- Layer Stackup
- Via Models
- Design Rules
- Signal Integrity.

By making initial decisions in these areas, the task of finding a breakout solution becomes feasible as opposed to overwhelming. For purposes of this paper, a specific set of values that work well together for large pin-count BGAs has been chosen for these variables.

**Stackup and via models**

The choice of stackup and via models will have the greatest impact on reducing layer count. Of course there will be exceptions to the recommendations in Figure 2 and the data in the chart should be considered as guidelines. What happens if one tries to use a borderline via model and stackup? Design rules (smaller feature sizes and clearances) will have to be compromised, resulting in lower fabrication yields and potential crosstalk problems.

**Laminated versus buildup**

Buildup technology, also known as High Density Interconnect (HDI), has taken over the handheld industry and is the preferred stackup for all PCBs in the PAC Rim. However,
it still lags behind FR-4 laminated in the US and Europe for computer, network and larger designs in general. High pin-count and less than 1mm pin-pitch BGA will force the adoption of HDI for all PCBs. The good news is that HDI is now low cost and for the same pin density actually lower cost than laminated.

The stackup in Figure 3 is one that worked best with the Mentor team’s breakout attempts for the Virtex-4 and Virtex-5 series with 1760 pins. In the world of HDI, this stackup is common and cost effective:

- GND is on the outer layers and each signal layer has a good reference plane next to it. Having the GND on the outer layers also provides excellent control of EMI.
- There are 4 signal layers, which is enough for the breakout. More signal layers can be added in the centre of the stackup if required.
- The 11-12 and 10-12 vias are not used for the signal breakouts, but may be used for power and ground if bypass capacitors are needed. Some FPGAs like the Virtex-4 and Virtex-5 series have bypass capacitors in the BGA package, minimising the need for them on the PCB under the device.
- The signal layers are not paired; rather they are separated by GND planes. The breakout traces on a large BGA usually result in layer-to-layer parallelism. Using GND planes between the layers eliminates the crosstalk potential.

**Design rules**

Only two criteria drive design rules; obtaining high fabrication yields (cost) and fulfilling signal integrity requirements (performance). Of course a third could be “what we have done in the past” as a justification to ignore the first two; fortunately, the number of companies wrapped up in that praxis are few.

For signal integrity purposes, it is generally desirable to have 50 ohm traces for single-ended nets and 100 ohm traces for differential pairs. Using the HDI stackup shown in Figure 3, this can be attained by using the following design rules (values for English units are rounded off):

- Single-ended – width 0.13mm (5th), clearance 0.13mm (5th)
- Differential pairs – width 0.1mm (4th), clearance 0.15mm (6th), pair to pair clearance 0.3mm (12th)
- Layer 1-2 micro-via pad 0.25mm (10th), hole 0.1mm (4th)
- Layer 1-3 micro-via pad 0.3mm (12th), hole 0.15mm (6th)
- Layer 2-11 buried-via pad 0.4mm (16th), hole 0.2mm (8th)
- Ball pad 0.6mm (24th).

These design rules are also quite good for low fabrication cost since most PCB fabricators routinely produce boards with 0.1mm width and clearance.

Depending on the fanout and routing method used, it may be necessary to compromise these design rules inside the BGA. For example, to enable routing from the fanout vias to the perimeter of the device, it may be necessary for the single-ended routes to have a 0.1mm width and clearance. The consequence of this compromise is that you will have a small impedance discontinuity when the trace changes to 0.13mm – this may or may not be a significant problem in the context of all the other signal integrity effects being managed in the design.

**Signal integrity**

While creating the breakouts for the Xilinx Virtex-4 and Virtex-5 series FPGAs, the following signal integrity considerations were made:

- Reference planes - Common reference plane for all signals in the same bank. This was addressed by routing all the signals in the same bank on the same layer and by providing a good reference plane for each layer.
- Differential pairs - Routing the pairs as 100 ohm transmission lines, with similar length, appropriate compliment spacing, and sufficient clearance from other differential pairs to minimise crosstalk.
- Single-ended nets - Routing these nets as 50 ohm transmission lines, and providing sufficient clearance to other traces to minimise crosstalk.
- Buried via crosstalk - Some concern has been expressed over the potential for crosstalk between the buried vias in the HDI stackup and...
that the clearance between them should be more than 0.1mm. Investigation on this showed varied opinions and the question won’t be resolved until the appropriate simulations are run. One version of the breakout includes increased clearances between the buried vias of different differential pairs. However, this method forces the number of signal layers to be 6 instead of 4 because the fanout vias need to be staggered as opposed to aligned.

**Fanout via patterns**

After setting up the design to properly minimise fabrication costs and manage signal integrity, the fanout via patterns have the most significant effect on the number of layers for the breakout.

**Thru-vias** - If thru-vias in a laminate structure must be used, then there really are only two options when the pin-pitch is 0.1mm. The vias must be placed either in the centre between the ball pads or in the pad (which increases the fabrication costs because the via must be filled and the ball pad smoothed prior to assembly).

**Micro-vias** - Using micro-vias in an HDI stackup is essential to reduce layer count. In the context of the Figure 3 stackup, the number of breakouts created with the 1-3 via should be maximised. Doing this opens up considerable routing space on the other 3 routing layers because the 1-3 via doesn’t exist as shown in Figure 4.

If the 1-3 fanout vias are aligned in a pattern as shown in Figure 5, additional routing space is created compared to just having a matrix of vias on 1mm spacing.

**Micro-vias plus buried-vias** – To get to the routing layers 5, 8 & 10 requires the use of a 1-2 fanout micro-via and a layer 2-10 buried-via. Again, a good fanout pattern is needed to maximise the routing space. In Figure 6, an effective pattern is shown.

If it is necessary to increase the clearance between the buried vias to minimise crosstalk between differential pairs, the vias can be staggered as shown in Figures 7 and 8.

Each large pin-count BGA presents different problems for fanout patterns and because of this, it is likely that a different fanout pattern will be required. The following factors and their combinations may cause unique fanout patterns to be used:

- **Arrangement of power and ground pins** - Sometimes they are grouped in the centre, other times sprinkled around the device in regular or irregular patterns that could interrupt the ability to use the same fanout pattern for the I/O pins.
- **Arrangement of the banks on an FPGA** - The banks may be grouped together nicely or sometimes split up. The arrangement of the pins in the bank may or may not be convenient for differential pair routing, especially since the use of aligned or staggered micro-vias and buried-vias tend to warp the nice symmetry that is often provided at the ball pad level as shown in Figure 9.
- **Extremely dense BGAs** - In Figure 10, you can see the areas that are easy to breakout (green) and the difficult areas (red). To breakout the red areas using minimum layers on a very dense BGA will require contortion of the fanout via patterns simply because there is so little available space and each area needs to be customised as is the case with any very dense PCB routing. This is illustrated in the alternating via patterns shown in Figures 11 thru 12.

**The tipping point**

BGAs will continue to grow in pin-count and density. At 1mm pin-pitch it is still feasible to use laminated PCB technology with thru-vias and/or blind and buried vias. However, if it is necessary to minimise layers, using HDI with micro-vias is the best method. Once the BGA packages have more than 2000 pins and a pin-pitch of 0.8mm, HDI will be required. Now is a good time to get ready for this change.

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