PWB/Component Materials And Finishes: A Pb-Free Analysis

by the Massachusetts Lead-Free Research Consortium, University of Massachusetts

The worldwide movement to phase out Lead from electronic products presents challenges for companies throughout the electronics supply chain. Because Lead had been integral to the integrity and reliability of electronic products, it is necessary to make changes carefully, and with the full participation of all parts of the product supply chain. The University of Massachusetts Lowell and the Massachusetts Toxics Use Reduction Institute have brought together several key companies in the Commonwealth to form a research consortium to investigate Lead-free manufacturing.

Figure 1 - Test vehicle

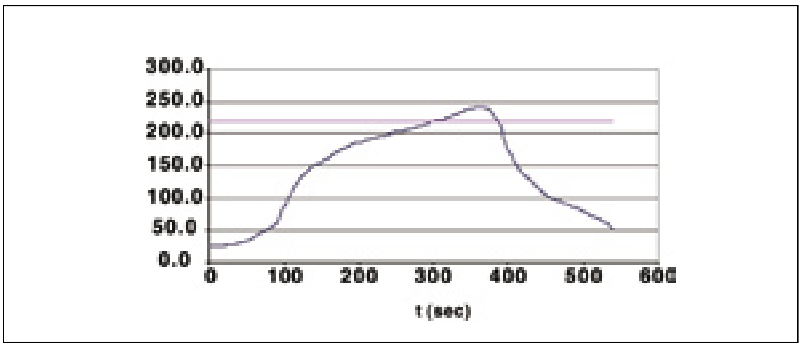


Figure 2 - Reflow profile for SMT board assembly

In January 2003, The European Union published Directives 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE) and 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS). These emerging directives have been the primary drivers for global movement toward Lead-free electronics. The RoHS prohibits products that contain Lead to be sold in the EU after July 2006, unless the use is specifically exempted. The second major influence has been the movement of electronics manufacturers, particularly Japanese companies, toward so called "green products."

Massachusetts Lead-Free Consortium

The Massachusetts Toxics Use Reduction Act (TURA) program has a mission to assist companies in reducing or eliminating the use of toxic substances where possible, and in reducing the amount of toxic waste generated. TURA also has a goal "to sustain, safeguard and promote the competitive advantage of Massachusetts businesses, large and small, while advancing innovation in toxic use reduction and management." These goals come together as TURA assists firms in meeting international materials restrictions on Lead in electronic products.

The Massachusetts Lead-Free Research Consortium was formed in 2000, consisting of at least one representative of each part of the electronics supply chain. Current consortium members are Tyco Electronics, Texas Instruments, Raytheon, Schneider Electric, BTU International, Air Products and Chemicals, Analog Devices, UML and TURI.

Experimental design

A design of experiment matrix was selected by the consortium members based on their collective experience and the available resources and materials. The factors and levels selected were as follows:

1) PWB finishes (five treatments): Solder Mask Over Bare Copper with Hot Air Solder Leveling (SMOBC/

HASL), Matte Finish Tin (Sn) Electroplate, Immersion Silver (Ag), Organic Solder Preservative (OSP), and Electroless Nickel Immersion Gold (ENIG).
2) Reflow atmospheres (two treatments): air and Nitrogen. Nitrogen was supplied by Air Products and Chemicals and contained 50 ppm Oxygen for these experiments.
3) Solder pastes (three treatments): all with the same alloy composition – 95.5Sn-3.8 Ag-0.7Cu (NEMI recommended) from three different suppliers (A, B and C), all incorporating no-clean fluxes.
4) Component lead finishes (four treatments): matte Tin plating, Tin/Silver/Copper, Nickel/Palladium/Gold, and Nickel/Gold.
5) Sn-Pb eutectic solder PWB using the solder treatments as control PWBs.

Source	DF	Sum of Squares Mean	Square	F Value	Pr > F
PWB Finish	4	44.7	11.2	7.33	0.0003
Solder	2	79	39.5	25.91	<.0001
Atmosphere	1	132.4	132.4	86.88	<.0001
Finish * Solder	8	16.04	2.00	1.32	0.2735
Finish* Atmosp.	4	15.3	3.8	2.51	0.0629
Solder * Atmosp.	2	54.3	27.2	17.83	<.0001
Finish * Solder *Atmosphere	8	21.8	2.7	1.79	0.1184
Total	59	409.20			

Table 2 - Statistical analysis – total visual defects

Figure 3 - Position of QFP pulls

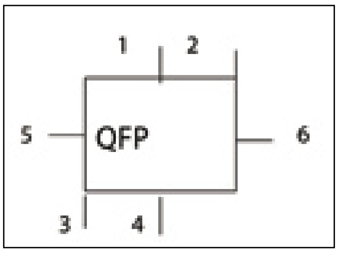
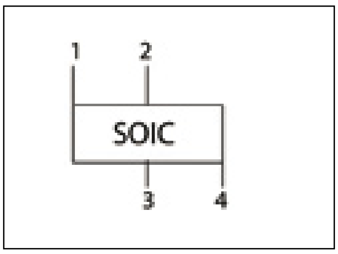


Figure 4 - SOIC pulls



Test vehicles and experimental plans

The test vehicle was a 152 x 228mm FR4 board, shown in the pull test fixture (Figure 1). A total of 100 PWBs were assembled and tested. The PWBs were divided as follows:

1) 60 PWBs consisting of 2 sets of 30 to harness the full factorial experiment of 5 finishes, 3 solder suppliers and 2 atmospheres (5 x 3 x 2 = 30). The full factorial experiment is shown in Table 1.
2) 10 PWBs, consisting of 2 sets of 5 PWBs soldered with a leaded solder from supplier B to act as baseline comparison to unleaded solder.
3) 8 PWBs, consisting of 2 sets of 4 to test out a more concentrated percentage of Nitrogen (50 ppm versus 5000 ppm oxygen).
4) 20 PWBs, consisting of 2 sets of 10 PWBs, to compare the results of leaded and unleaded components versus leaded and unleaded solders, using all 5 PWB finishes, air soldering environment and solder supplier B. This set was performed to demonstrate whether it is possible to exchange unleaded components with leaded components at will in all soldering environments.

Components

The control PWBs were built with devices that had a Tin/Lead component finish and the experimental test boards were assembled with parts that had Lead-free finishes. The Lead-free passive chips were Tin-plated and the Lead-free integrated circuit devices were plated, some with matte Tin plating, Tin/Silver/Copper, Nickel/Palladium/Gold, and Nickel/Gold.

Each PWB included:
1) Standard SMT resistor and capacitor parts. (401 and 402 styles)
2) A set each of 0.76 and 0.35 mm vias
3) 3 QFP 176 high-density interconnection (HDI) package one with daisy chain terminations
4) 2 BGA types, 35 and 45 mm
5) 3 SOIC 20 packages, one with daisy chain terminations
6) 3 special ICs used in wireless applications

Experiment layout

The test PWB was laid out taking into account daisy chain resistance test capabilities in some of the parts and fabricated with the five different finishes. Pastes were obtained from three vendors and a reflow profile was developed based on the manufacturers' product data sheets. A reflow profile board was populated with parts and three Kprobe thermocouples (TC) were attached to the surface. One TC was attached at the leading edge of the PWB, one at the lead attach area of a large QFP and one near the trailing edge. The thermocouples were connected to an industry standard data logger. The thermal readings were downloaded to the data collector software for comparison to the manufacturer recommended profiles. All three manufacturers recommended a 'ramp to spike' curve. The reflow profile used for all three Pb-free solders is shown in Figure 2.

Solder paste prints were made using a 0.152 mm thick stainless steel laser cut, electropolished stencil. Ten percent aperture reductions were used on the fine pitch devices. After reflow, PWBs were packaged in ESD bags. Inspection criteria were established as follows: Total Defects, Cold Solder joints, Non-wetting, Solder Balls, Dewetting, Bridging, Pinholes, Shiny Appearance, Smooth Appearance, and Flux Residue. X-ray radiography of the BGA solder joints was also performed. Initial inspection data has been tabulated and statistically analysed.

Visual defects statistics

Eight main categories of common defects were selected and all boards were inspected. Statistical analyses were performed using Minintab and the significant effects shown in Table 2 were determined.

Pull test analysis results

The test methodology consisted of using an Instron pull test machine to pull the leads of an IC at different positions and record the maximum pull force. For the QFP (Nickel/Palladium/Gold) components leads, 6 leads were pulled as follows (Figure 3), and for the SOIC 20 (Nickel/Palladium/Gold) and the SOIC 16 (Tin plate) component leads, 4 leads were pulled (Figure 4).

QFP-176 and SOIC-20 pull test results

The leads of the QFP-176 and SOIC-20 devices that were pulled had a Nickel/Palladium/Gold finish. 6 pulls were made for each of the 30 QFPs in the full factorial experiment shown in Table 1, for a total of 168 pulls. Four pulls were made for each of the 20 SOICs for a total of 112 pulls. The ANOVA analysis for QFP is shown in Table 3 and for the SOIC in Table 4. The QFP factor pulls averages are shown in Figure 5, and the lead free average analysis - SOIC 20 - is shown in Figure 6.

Comparison of unleaded vs. leaded solder and QFP compments is shown in Figure 7.

Factorial experiment analysis for QFP and SOIC pulls

Some of the conclusions that can be derived from this full factorial analysis from Tables 3-4 and Figures 5-6 are as follows:

1. Since all leads have a Nickel/Palladium/Gold finish, these conclusions are applicable to this case.
2. The pull force in the SOIC was significantly higher than QFP due to the large solder surface area in the IC pads.
3. The surface finish has a significant effect on the pull test of the leads. Of the five finishes (SMOBC, OSP, ENIG, Matted Sn and Imm AG), the analysis showed that ENIG was significantly lower than the other finishes in both IC's pulled. Finish 2 (OSP) was significantly higher in QFP and Finish 1 (SMOBC/HASL) was significantly higher in SOIC.
4. The solder suppliers were not important in the pull tests for the 2 IC types. Supplier B (Indium) was slightly higher in QFP-176 and significantly higher in SOIC-20.
5. Nitrogen was significantly higher than air reflow for QFP-176, not significant for SOIC 20
6. Some of the interactions were significant, more so in QFP than SOIC 20.

Experiment #	Surface Finish	Solder paste	Atmosphere
1	SMOBC/HASL	"A"	Air
2	SMOBC/HASL	"A"	Nitrogen
3	SMOBC/HASL	"B"	Air
4	SMOBC/HASL	"B"	Nitrogen
5	SMOBC/HASL	"C"	Air
6	SMOBC/HASL	"C"	Nitrogen
7	OSP	"A"	Air
8	OSP	"A"	Air
9	OSP	"B"	Nitrogen
10	OSP	"B"	Air
11	OSP	"C"	Nitrogen
12	OSP	"C"	Air
13	ENIG	"A"	Nitrogen
14	ENIG	"A"	Air
15	ENIG	"B"	Air
16	ENIG	"B"	Nitrogen
17	ENIG	"C"	Air
18	ENIG	"C"	Nitrogen
19	Matte Sn	"A"	Air
20	Matte Sn	"A"	Nitrogen
21	Matte Sn	"B"	Air
22	Matte Sn	"B"	Air
23	Matte Sn	"C"	Nitrogen
24	Matte Sn	"C"	Air
25	Imm. AG	"A"	Nitrogen
26	Imm. AG	"A"	Air
27	Imm. AG	"B"	Nitrogen
28	Imm. AG	"B"	Air
29	Imm. AG	"C"	Air
30	Imm. AG	"C"	Nitrogen

Table 1 – Lead-free full factorial solder test plan

Unleaded vs. leaded solder baseline for QFP-176 and SOIC-20

For each of the 5 surface finishes, a PWB was reflowed with the leaded solder from supplier B in air, which was used as the baseline for comparing pull tests. Figures 7 and 8 show the comparisons for QFP and SOIC respectively. All components used had Nickel/Palladium/Gold finish.

Since Nitrogen was significant in QFP-176, only air soldered PWBs from each finish (3 PWBs for each of 5 were used in the comparison for QFP. For SOIC-20, all PWBs (6 PWBs for each of 5 finishes) were used in the comparison to the leaded solder baseline. The comparisons were made using a multiple-range test for means. Unfortunately the baseline PWB for Im-

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Surface	4	5.36	1.34	5.0	0.001
Solder	2	1.7	0.85	3.17	0.045
Atmosphere	1	4.32	4.32	16.10	0.000
Surface* Solder	8	18.6	2.33	8.68	0.000
Surface*Atmosp	4	1.04	0.26	0.97	0.428
Solder *Atmosp.	2	3.0	1.5	5.57	0.005
Error	146	39.1	0.2681		
Total	167	73.7			

Table 3 - Statistical analysis – QFP pull test (6 Pulls/IC)

Source	DF	Sum of Squares	Mean Square	F Value	Pr > F
Surface	4	77.0	19.30	7.35	0.000
Solder	2	17.721	8.860	3.38	0.038
Atmosphere	1	1.758	1.758	0.67	0.415
Surface* Solder	8	14.258	1.782	0.68	0.707
Surface*Atmosp	4	28.720	7.180	2.74	0.033
Solder *Atmosp.	2	9.970	4.985	1.90	0.155
Error	90	235.6	2.618		
Total	111	392.804			

Table 4 - Statistical analysis – SOIC pull test (4 Pulls/IC)

mersion Silver (AG) leaded solder was not available. The analysis had to be performed separately for QFP-176 and SOIC-20 because of higher pull force for SOIC.

For all B leaded solder pastes used as baseline and air reflowed; the QFP-176 leads showed no significance due to PWB surface finish. The SOIC-20 leads showed that ENIG was the only significant (lower) pull force.

1. Unleaded and leaded pull tests showed no significant differences if the same solder supplier (B) provided the solder paste, except for QFP ENIG and SOIC SMOBC. Otherwise the solder supplier proved to be a significant difference. This might indicate that other factors such as solder paste formulation might play a role in making a significant difference between leaded and unleaded solder, more so in smaller footprint ICs such as QFP.

2. When comparing leaded solder supplier (B) with all 3 unleaded solder suppliers, some significant differences arise. These are shown in Table 5 for homogenous group in the same column. For Immersion Silver (AG), the comparison was not possible since the baseline data were not recorded because of manufacturing problems with the sample PWBs.

Table 5 is an attempt to separate the data for each component type, solder supplier and PWB finish and shows the pairwise comparison of all samples in a statistical technique called Multiple Range Tests. This technique is a method to divide samples into groups which are homogenous to each other (not significant), but may be significantly different than other samples within the group.

Compatibility of leaded/unleaded solders vs. leaded/unleaded components

This test was performed for Tin plated SOIC 16 components to determine whether it was significant that leaded and/or unleaded solder and/or components with Tin plat-

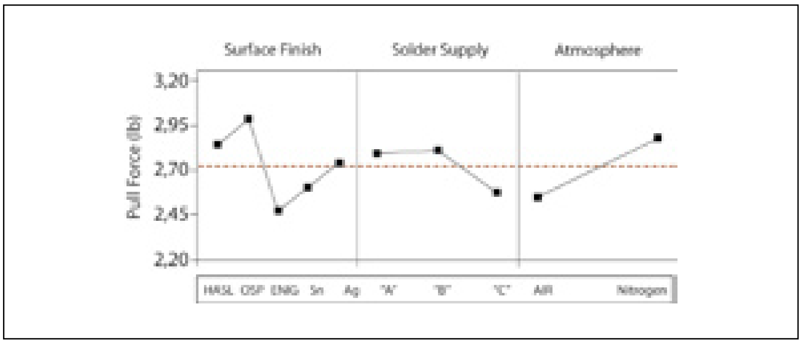


Figure 5 – Pull test Lead-free average analysis – QFP

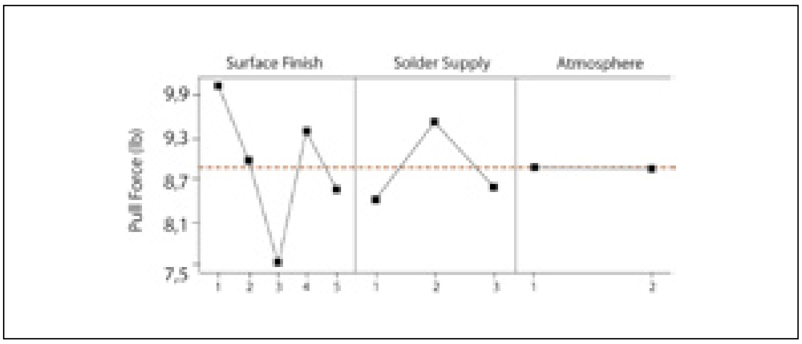


Figure 6 – Lead-free average analysis – SOIC 20

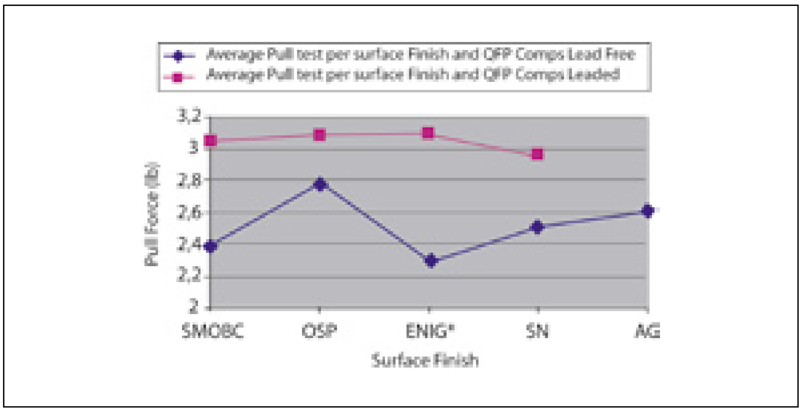


Figure 7 – Comparison for unleaded vs. leaded solder and QFP comps

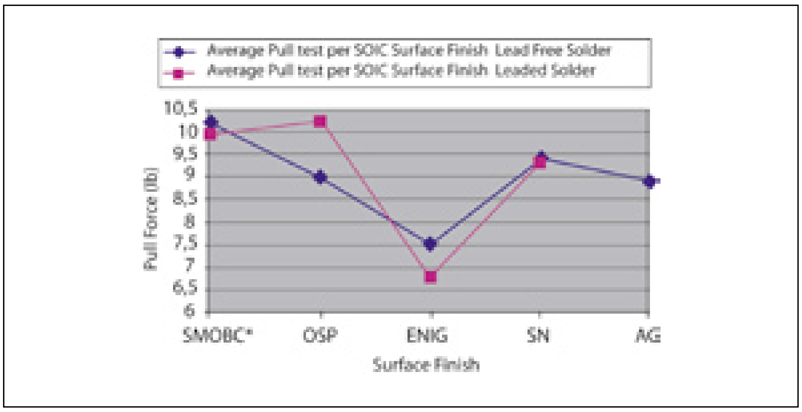


Figure 8 – Comparison of unleaded and leaded solder per PWB surface finish and SOIC comps

Comparison of unleaded solders to leaded baseline Nickel/Palladium/Gold Lead Finish			
QFP - SMOBC PWB Finish		SOIC 20 – SMOBC PWB Finish	
X	(C solder, pb free)	X	(B solder, leaded)
X	(B solder, leaded)	X	(C solder, pb free)
X	(B Solder, pb free)	X	(B solder, pb free)
QFP - OSP PWB Finish		SOIC 20 - OSP PWB Finish	
X	(A Solder, pb free)	X	(C solder, pb free
XX	(C Solder, pb free)	XX	(A solder, pb free)
X	(B solder, leaded)	X	(B solder, pb Free)
X	(B solder, pb Free)	X	(B solder, leaded)
QFP - ENIG PWB Finish		SOIC 20 - ENIG PWB Finish	
X	(B Solder Lead free)	X	(B solder, leaded)
XX	XX (C Solder, pb free)	X	(B solder, pb free)
XX	XX (A Solder, pb free)	X	(C solder, pb free)
X	X (B Solder, leaded)	X	(A solder, pb free)
QFP - Matte SN PWB Finish		SOIC 20 - Matte SN PWB Finish	
X	(C Solder, pb free)	X	(B solder, leaded)
X	(A Solder, pb free)	X	(B solder, pb free)
X	(B Solder, leaded)	X	(C solder, pb free)
X	(B Solder, pb Free)	X	(A solder, pb free)
QFP - Imm Ag PWB Finish		SOIC 20 - Imm AG PWB Finish	
X	(B solder, pb free)	X	(B solder, pb free)
X	(C solder, pb free)	X	(C solder, pb free)

Table 5 - Multiple range tests – homogenous groups

ing finish can be used for different types of PWB surface finish. This will enable component customers to achieve forward and backward compatibility as the industry transitions to Lead-free technology. The results are shown in Table 6, for the 7 combinations of solders and component-finishes tested. There were no significant differences in the 21 (6+5+4+3+2+1=21) pair-wise comparisons made. The baseline set of leaded solder and leaded component-finishes, and the ultimate goal of unleaded solder and unleaded component-finishes was not fabricated.

Conclusions

This research has shown the effects of atmosphere, paste selection, and PWB surface finish on visual appearance defects and an initial reliability assessment of Lead-free soldering. While Nitrogen and paste "B" yielded the fewest visual defects and SMOBC

• HASL was significantly worse as a surface finish, the assembly process was not optimised for any of the variable options. Further, throughput and cost can be significant issues that may override some of these results. For pull testing, this research established several important conclusions:

• The selection of materials and process affects the pull strength of the solder joints for the QFP and SOIC components tested, using components with Nickel/Palladium/Gold finish: The pull forces are dependant on the footprint of the components used. Thus pull forces in the SOIC were significantly higher that QFP. The PWB surface finish has a significant effect on the pull test of the leads. Of the five PWB finishes (SMOBC, OSP, ENIG, Matted Sn and Imm AG), ENIG was significantly lower than the other finishes in both IC's pulled. OSP was significantly higher in QFP and SMOBC/HASL was significantly higher in SOIC. The solder suppliers were not important in the pull tests for the two IC types. Supplier B was slightly higher in QFP and significantly higher in SOIC 20. Nitrogen was significantly higher than air reflow for QFP, not significant for SOIC.

• Comparison of unleaded solder pulls to leaded solder pulls in QFP and SOIC, using components with Nickel/Palladium/Gold finish. This comparison was difficult since the baseline leaded PWBs were made with a single process: that of being soldered in air with leaded solder from supplier B, and the Silver surface finish baseline was not available. The data indicated that the difference is not significant in most cases when using the same solder supplier (B) for unleaded and leaded solders.

• Interchangeability of leaded and unleaded components and solders in SOIC and Tin plated components pull tests. This is an important issue for electronic component suppliers and customers, concerned about keeping a dual set of materials for different markets around the world as the technology transitions from leaded to Lead-free soldering. The data indicates that for the set of 7 conditions analysed in Table 6, with 21 pair-wise tests, there is no significant difference in the pull test results. Note that the baseline condition of leaded solders and component-finishes, and the ultimate condition of Lead-free solders and component-finishes were not tested.

Table 6 - Multiple range tests

Comparison of unleaded solders to leaded baseline with leaded and unleaded tin plated lead finishes.	
X	(AG, B pb free solder, leaded comps)
X	(AG, B leaded Solder, pb free comp)
X	(SN, B leaded Solder, pb free Comps)
X	(SN, B pb free solder, leaded Comps)
X	(SMOBC, B pb free solder, leaded Comp)
X	(ENIG, B pb free solder, leaded Comps)
x	(OSP, B pb free solder, leaded Comps)

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