Enabling Chemistries For 3D And Wafer-Level Packaging

by David Zoba and Russ Stapleton, Lord

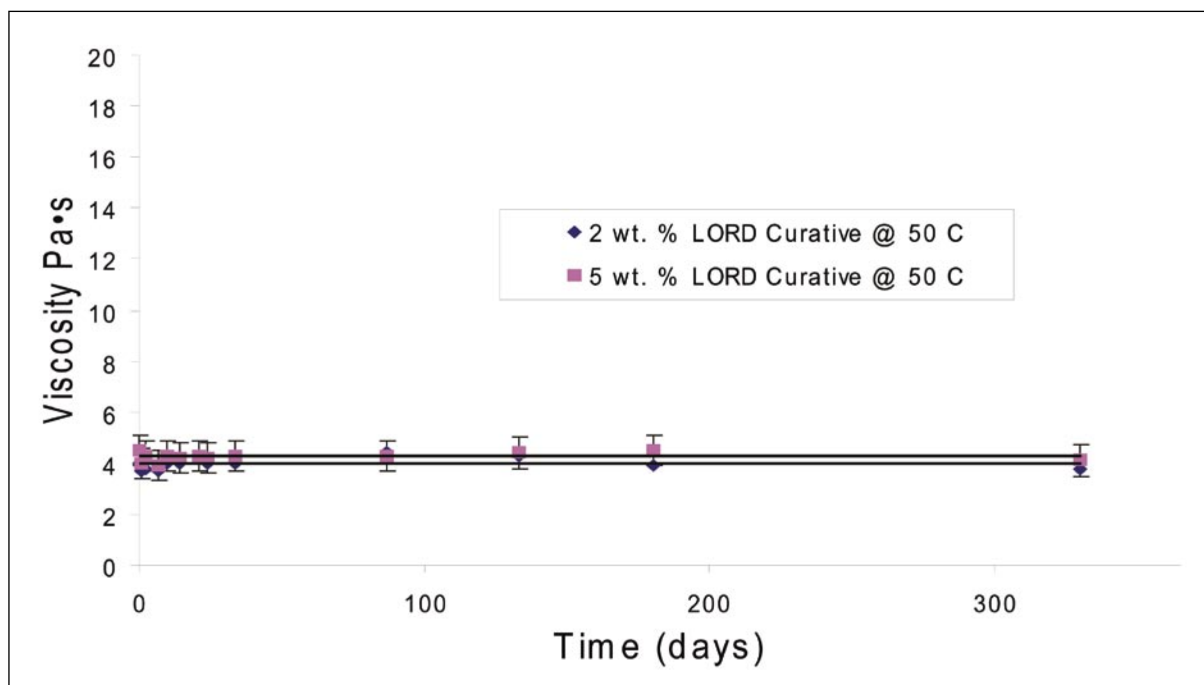
The future of wafer-level packaging, especially those concerns related to die stacking, cost, small footprint, thin bond lines, fine pitch and reliability, are dependent on the evolution of key chemical technologies that specifically address the needs of the package and process. By understanding the functional chemistry in line with the material needs, a true wafer-level-applied die protection solution can be developed to provide the next level of critical cost/performance options to packaging engineers.

Flip chip and chip scale packaging designs are bringing smaller and lighter devices to market, especially those that are portable and battery operated. However, the combination of consumable cost drivers, environmental demands and increased performance requires a greater emphasis on efficient and effective package designs. Wafer-level packages may soon offer economic solutions to chip scale packages (CSPs) and die stacked packages, as interposers are eliminated. Wafer-level chip scale packages (WLCSP) not only offer the advantage of economy of scale processing, but also potentially improved yield as testing occurs at the wafer level, so known good pre-packaged die are only used in assembly. Limitations in wafer-level packaging have been effected by the ability to adapt die/board-level processes and materials to the wafer.

Wafer-level packaging options for electrical routing already exist, including redistribution layers and bumping. One critical die to board-level packaging material that has not been adapted to the wafer is the underfill. Attempts to adapt underfill technologies to wafer-level processes have proven to be costly. Many of the front side die protection schemes used to date incurred additional processing/material costs and unacceptable yield losses. While capillary underfills and molding compounds will remain a mainstay of die protection, the evolution of advanced package designs will enable opportunities for wafer-level packaging, especially those related to die stacking, cost, small footprint, thin bond lines, fine pitch and reliability.

Much of the traditional underfill chemical technologies have been exploited and redirected towards wafer-level packaging, e.g. transfer molded wafers, but none have been successful in delivering a suitable product that would displace capillary underfills. In order to realize an effective wafer-level-applied die protection solution, it is important to understand the chemical technologies of front side wafer applied coatings. The chemical mechanism through which the coating is solidified, or cured, to meet the specific

Figure 1 – Epoxy/curative blend showing no viscosity change while being stored at 50°C for extended time. The stability of this curative/resin blend allows for excellent stability at ambient conditions



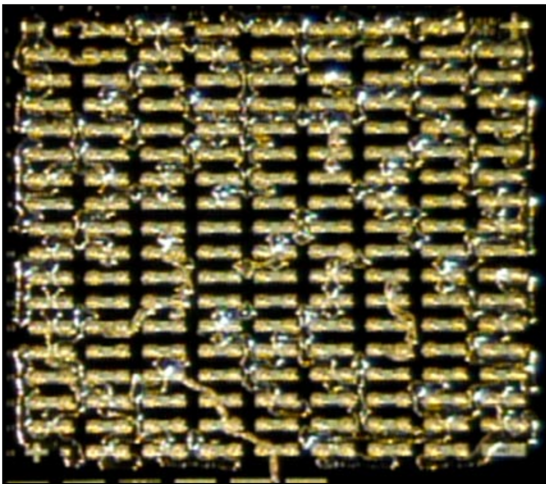


Figure 2 – The increase in viscosity from typical (or traditional) curatives has been shown to cause significant increases in void formation as the material ages

Figure 3 – The difference in the relative number of voids under the chip when a small amount of standard electronics resin and curative mixture was applied, observed through the glass slide, after the solder reflow

performance and cost requirements of wafer-level package designs is one of the key elements in making the transition to wafer-level protectants.

Understanding the chemistry

Front side protective coatings are typically applied as liquids or films. These materials are predominantly uncured epoxy formulations, and thus require a cure mechanism to achieve suitable property development (e.g. adhesion, glass transition temperature (Tg) and modulus). The most common curatives for epoxy resins are functionalized imidazoles or blocked imidazole adducts. Compared to amine cured epoxies, imidazoles deliver extended pot life at room temperature, while still providing fast cures when heated. Furthermore, imidazoles are superior to amines in reliability and moisture resistance as they do not contribute to the extractable halides or develop a corrosive environment.

The demands on the curative for a wafer-level coating exceed that of what imidazoles or any other existing curative technology can provide. A wafer-level coating must demonstrate viscosity stability for at least one year at room temperature. The material should also be insensitive to humidity, light, and ideally, completely cure during the very short lead-free solder reflow thermal profile. Lord recently created such a curative, specifically designed for epoxies cured during the lead free reflow cycle, which would be the case for a wafer-level-applied die protectant. The novel curative is also applicable for other adhesives, such as board applied fluxing adhesives.

The curative is based on a thermally degradable organic salt, which when heated in a 260°C lead-free reflow profile, initiates the polymerization of epoxies and similar resins. Unlike inorganic halide-based salts, the curative is hydrophobic and soluble in common packaging resins. Further, unlike most traditional curatives that achieve latency by limited solubility, a fully soluble curative disperses completely in the resin, therefore eliminating hot spots during the cure which can cause many voiding issues. The use of a polar, yet hydrophobic salt also helps keep humidity issues in the uncured and cured formulations from reemerging as voids and/or poor reliability. The new curative technology has been tested with a variety of resins to determine contributions to total residual corrosive ions or other reliability failure mechanisms. For example, a cured high-purity Bis-F epoxy with 1-5 percent curative shows no measurable increase in residual extractable ionics and no deleterious effects of corrosion or electro-migration have been observed.

Latency

In order to keep a WLCSP process cost-effective, it is desirable to maintain the packaging steps at the wafer level as long in the process as possible. A CSP wafer is coated with a wafer applied material. The coated wafer needs to be handled and stored for extended periods of time, making freezing of the wafers impractical. Therefore, it is critical for wafer applied materials to have extended room temperature latency and stability.

Such a coating material must not show any increase in viscosity or degradation during its application process. If the wafer-level coating advances in viscosity during storage, the variability in process performance of the package would lead to substantial yield loss. The curative technology achieves stability by having an extremely slow rate of reaction during room temperature storage as seen in Figure 1.

When the resin and curative mixture was stored at 100°C, the resin doubled in viscosity in two days and required about one week to gel. This open time performance at elevated temperatures is superior to any other latent technology used in underfill curing.

The increase in viscosity from typical (or traditional) curatives has been shown to cause significant increases in void formation as the material ages, as seen in Figure 2.

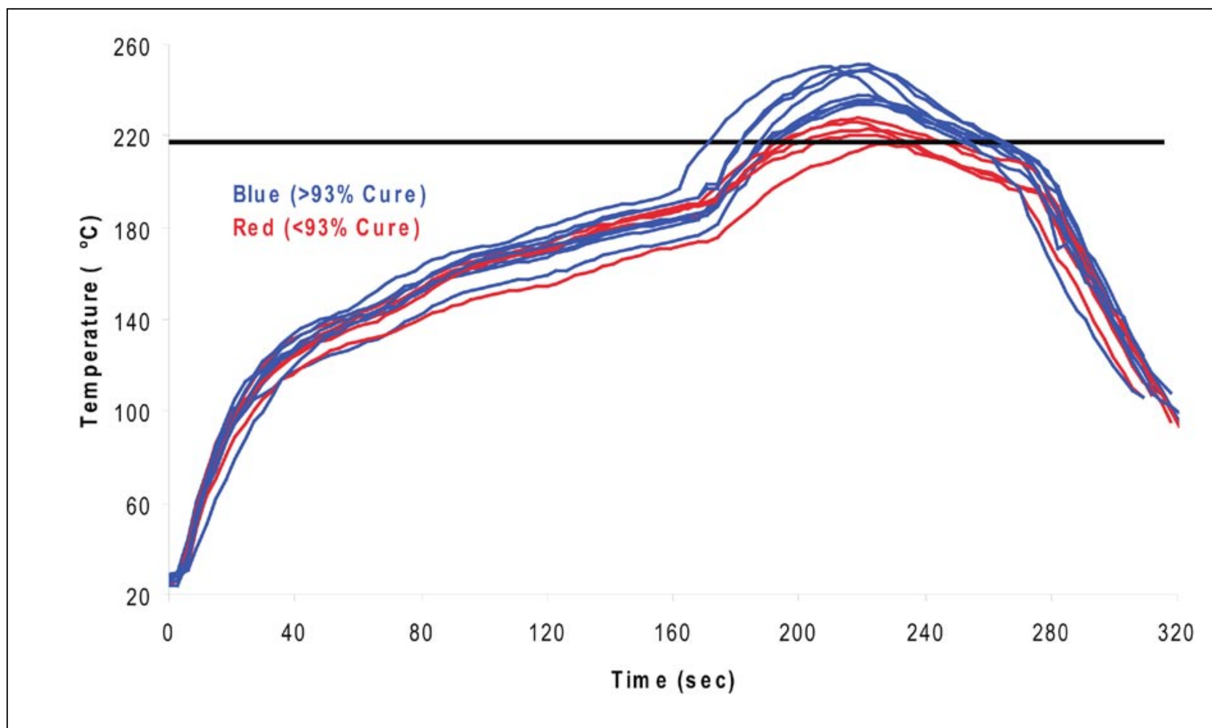


Figure 4 – Curing profile for epoxy/curative blends showing the minimum curing required in a reflow to achieve greater than 93% cure by DSC

To illustrate how effective a latent curative is, a small amount of standard electronics resin and curative mixture was applied to a glass slide, and a bumped flip chip die was then placed on top of the drop. The die/underfill/glass assembly was subjected to a lead-free solder reflow/cure profile. Figure 3 shows the difference in the relative number of voids under the chip, observed through the glass slide, after the solder reflow. The longer the standard resin and curative mixture was aged, the more voiding occurred during die placement and reflow. In comparison, the Lord resin/curative system displayed no aging issues during the time period of the experiment. Had the standard resin/curative been applied to a wafer, the wafer assembly yields would have been very poor, while the material with the Lord curative would have remained acceptable for the process.

Properties development

Lead-free solder reflow profiles are higher in peak temperature than their eutectic analogs. Typical Sn/Ag/Cu alloy bumps require reflow peak temperatures in excess of 250°C, and often higher. The chemical kinetics of all curative/resin systems, and the resulting ultimate material properties, depend on the reflow profile peak temperature and the activation energy of the curative. With complex multi-functional materials, such as wafer-level coatings and fluxing underfills, the material property development is often difficult to control, predict and tailor for applications that require consistency in high reliability applications.

Using the typical lead-free solder reflow profile with a 260°C peak, the Lord curative proves to be effective during the reflow cycle. Samples processed through these reflow profiles showed that any material with less than a 93% cure by Differential Scanning Calorimetry (DSC) did not develop the full glass-rubber transition temperature (Tg), also measured by DSC. Further, building of a library of reflow profiles allows a map of the in situ reflow kinetics for a standard bisphenol-F resin to be created. This cure map can then be used as a selection guide for the reflow solder type/package design. In this way, the solder profiles show the minimum cure time at the 260°C reflow that must be maintained for proper properties development (Figure 4).

The kinetics of resin cure also translate to material property development. The performance of a curative can be gauged by its Tg development. High Tg materials that retain good adhesion in a reflow oven cans be difficult to achieve, more so than low Tg materials. Testing the curative on an unmodified bisphenol-F resin, Lord's curative technology is able to generate Tg values of 125°C in the reflow cycle.

Next steps

In order to deliver the performance requirements for advanced wafer applied materials, novel curatives are needed. This new curative was developed to cure epoxy-based materials during a 260°C lead-free solder reflow profile. It specifically addresses the shortcomings of commercially available curatives, by having low ionics, decreased moisture sensitivity, extended thermal stability, and minimal cure times in the reflow profile. Formulations developed with this curative have demonstrated complete cure during the solder reflow cycle with no compromise in material property development, thereby eliminating the need for a post bake step.