Electrical Feed-Through Wafers For MEMS Packaging

Wafer-level packaging of MEMS devices using cap wafers which include cavities and vertical electrical vias is an alternative to integrated encapsulation processes. This approach also enables the development of innovative MEMS solutions and can simplify the packaging of existing solutions. We take a look at the uses and benefits of Silicon and glass high via density electrical feed-through wafers for the manufacture of compact microsystem devices.

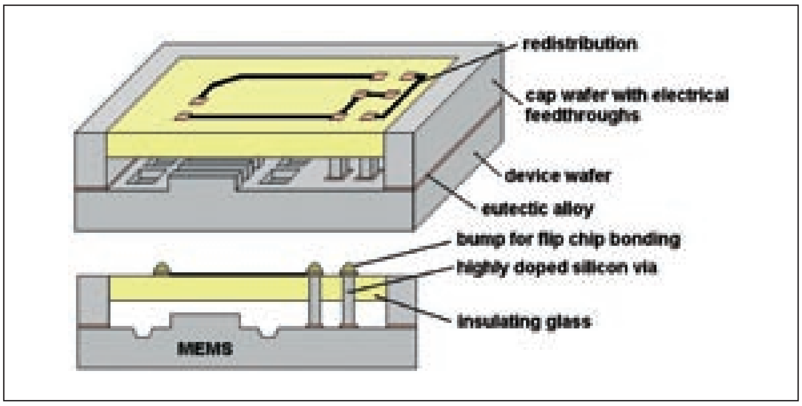

Figure 1 - Example of a packaged device using a cap wafer with vertical electrical feed-throughs

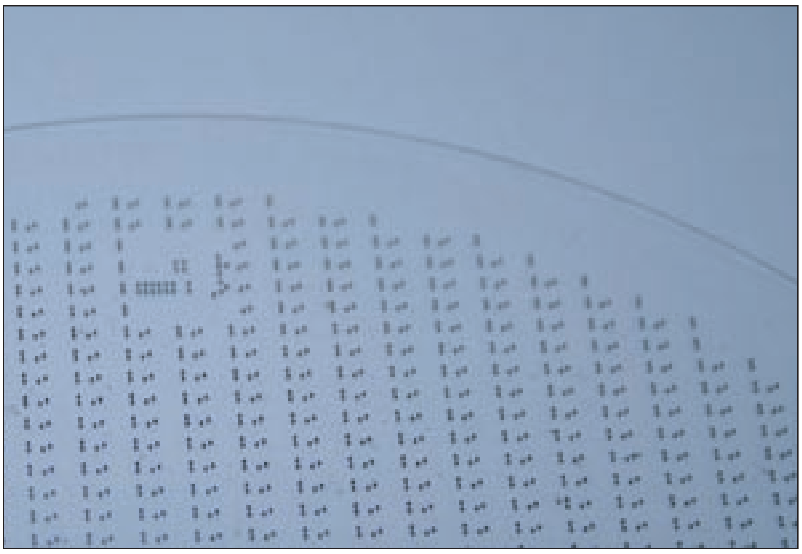

Figure 2 - An example of a feed-through wafer: glass wafer with conductive vias

The role of packaging

The packaging of Micro-Electro-Mechanical Systems plays an important role in the development of a device and must be investigated early on in the design phase. One of the main functions of packaging is to protect the device from the external, sometimes extremely harsh, environment. Another function is to provide mechanical support and electrical connections between the device and the outside or the next level of assembly. In addition, it is often necessary to achieve vacuum-sealed encapsulation. In particular, for micromechanical or freely moving parts, cavity sealing is absolutely vital. In this case, the electrical connections are often a challenge and require device-specific solutions. The goal of packaging is also to combine MEMS and other components like ASICs at the next level of assembly or perhaps into a final product. Furthermore the packaging has to guarantee the reliability and long lifetime of the product.

Packaging techniques

One method of packaging, which is becoming more significant, is wafer-level packaging (WLP). In this approach, the device wafer is bonded with a cap wafer using wafer-to-wafer bonding processes and separation of the dies by sawing is performed after the sealing process. This approach maximises the protection of the devices and enables easier handling in the subsequent assembly steps.

Novel feed-through wafers (Figure 1) offered by the German company Plan Optik provide device protection and vertical electrical connections at the same time. Among the advantages of these cap wafers is the possibility of etching cavities into the substrate without changing the shape or length of the feed-throughs, as well as easy redistribution of contact pads on the backside of the wafer.

Glass insulates the conductive vias that cross the Silicon wafers. The possibilities of such Silicon-glass compound wafers are shown in Figure 3. In addition to electrical feed-throughs, redistribution lines and glass areas providing a cavity can be achieved. Figure 2 shows a

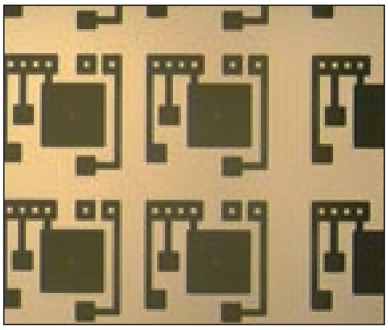

Figure 3 - Silicon-glass compound wafer with conductive vias, insulating redistribution lines and glass areas for cavities

glass wafer with vertical conductive vias. Borosilicate glass, which is anodically bondable to Silicon, is applied. The coefficient of thermal expansion (CTE) is adapted to Silicon to prevent thermal stress on the finished device. Common eutectic alloys can be used for the bonding of cap and device wafers. Assembly by TAB or wire bonding and in particular by flip chip is possible after dicing of the wafer.

The vias are made of highly-doped Silicon with a resistance of 1 Ohm or less. The minimum dimension of the feedthroughs and also the minimum isolation width can be less than 50 microns. The typical wafer thickness is in the range of 250 to 500 microns.

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Advanced Chip-To-Wafer Technology Agreement

EV Group and Datacon Technology have announced the installation of an EVG540C2W System at Datacon. During the long-term cooperation and development agreement in the field of advanced-chip-to-wafer (AC2W) technology, Datacon will enrich their application lab with EVG equipment. AC2W technology combines Datacon´s chip-bonding and key flip-chip bonding technologies with the wafer-level know-how from EV Group. During the initial phase, which starts with the R&D project, the technology offers high device density through stacked devices, short interconnects and higher functional density for applications. It also provides advantages for chip manufacturers, enabling the integration of various device processes such as hybrid integration of IC and MEMS functionality.

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MEMS/MOEMS 2D/3D X-Ray Inspection System

Comet announces an enhancement to the Feinfocus CT-Fox series of x-ray inspection systems: the Feinfocus HDCT-Fox. The new 2D/3D X-ray inspection system combines high-resolution 2D x-ray technology and enhanced 3D computed tomography techniques with proprietary Feinfocus HDx-ray technology for detailed inspection and analysis of complex electronic devices in the 3rd dimension. Capturing the sharpest high-resolution 3D imagery available, the HDCT-Fox is ideal for thorough inspection of applications requiring high magnifications, such as MEMS/MOEMS, semiconductor packages, high-density interconnects, and hybrids.

The new system combines the functionality of a standard microfocus x-ray system with the ability to generate 3D imagery. Utilising Feinfocus HDX-ray technology, the system instantaneously captures high-resolution 2D images and reconstructs 3D volume models with film-like quality, providing valuable insight into design and manufacturing processes. A modular hardware- and software-based CT interface accommodates a variety of imaging chains, with automatic configuration of the detector for optimal CT resolution.

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