The trends of increased functionality and reduced size of portable wireless products, such as handsets and PDAs, are demanding increased routing densities for printed circuit boards. The handheld wireless product marketplace demands products that are small, thin, low-cost, lightweight and with improved user interfaces. In addition, the convergence of handheld wireless phones with palmtop computers and Internet appliances is accelerating the need for miniaturised functional circuits designed with low-cost technology. We take a look at an evaluation conducted as a part of a phone product qualification build to ensure the stability of vias throughout the reflow process.

Historically, the industry has met the challenge of manufacturing high-functionality reduced-size electronic devices through high density interconnect technology and increased Silicon integration and component miniaturisation. Microvia high density interconnect (HDI) also known as build up technology, is one method for constructing circuit boards with high routing density.

For HDI board, vias can be formed using unreinforced dielectric such as Resin Coated Foil (RCF) and processing techniques such as laser drilling or photoimaging. The vias are then metallised using electroless Copper / electrolytic plating.

The advantage of the HDI construction is the ability to create smaller vias (150 micron) and via pad sizes. This enables higher routing density, lower metal count, reduced board area and increased functionality as compared to conventional boards. Past board technologies used at Kyocera-Wireless Corporation used single stack of microvias on the outer layers. (Layer 1-2 and Layer 7-8). Current phone technology boards have stacked microvias, Layer 1-2 and layer 2-3. Additionally, these vias are filled with electroplated Copper while the single stack vias were plated, but not filled.

**PWB design and fabrication**

Higher density packages and PWB applications requirements are driving the need for high-density interconnect design capabilities using microvias. The benefit of using HDI outer layers is the ability to incorporate high density, high performance area array packages to increase performance of handsets, PDAs etc.

Microvias are typically formed on an epoxy-resin laminate or dielectric layers on a core substrate and take up configurations such as 2-2-2 or 3-2-3, where the stack up configuration xx-yy-xx means xx layers of build up substrate and yy layers of core substrate.

Stacked microvia technology is emerging in industry, however, and production level reliability data for double-sided surface mount assembly is not readily available. This requires users to establish their own reliability data.

The PWB was designed as an 8 layer thin board 0.8 mm thick. The PWB had a combination of single and stacked microvias. The stack-up configuration was 2-4-2, with the outer two layers on top and backside of the PWBs made up of stacked microvia configuration. The microvias (150 micron diameter) were laser drilled and Copper plated and filled. Typical via configuration is shown in Figure 1(a) and (b).
Board assembly

Board assembly process was a double-sided surface mount assembly soldering of ball grid array packages, connectors, chip resistors, capacitors, diodes, etc. The assembly was then reflowed in a convection air furnace at a peak temperature of 219°C.

Post reflow cross-sections

Cross-sections were performed on the BGA packages and other components to evaluate the quality of the solder joints and ensure compliance to IPC 610 – Rev C for leaded packages and IPC 7095 for BGA packages. Also microvia integrity was evaluated with cross-sectional analysis.

Cross-sections showed acceptable solder joints and no degradation of microvias. Examples of the X-ray and cross sectional analysis are shown in Figures 2 and 3.

Rework evaluation

Rework of SMT packages is performed using hot air soldering tools and application heat using controlled ramp/soak profile. The concern was damage to microvia connections and PWB pads during component removal and reattach. Component rework was performed 2 times on the leaded packages and 1 time on the Ball Grid Array packages. All packages survived rework. There was no damage to PWB pads, or blistering of solder mask during rework. No damage was seen on microvia connections.

Shear testing

Shear testing was performed on SMT packages, post reflowing and after thermal shock to evaluate degradation of solder joints as a part of assembly qualification test. Results are shown in Figure 4. Shear values were within the acceptable range.

Solder joint reliability test

Solder joint reliability testing was performed for assembly qualification per IPC SM 785. Assemblies were thermal shock tested from -25°C to +125°C for 500 cycles. Temperature humidity testing was performed at 85°C/85% Relative Humidity for 500 hours. Samples were X-sectioned post test to evaluate the joint quality.

The joints appeared slightly grainy after thermal shock test and oxidised after temperature and humidity testing, but no cracks were seen in the joints. Average shear values post thermal shock was slightly lower than post reflow. A summary of the shear test results is shown in Figure 5.

Phone level drop test

Phone level drop tests were performed at 1.5 meters on a hard vinyl surface. Assemblies were cross-sectioned post drops to evaluate solder joints and microvia connections. No solder joint failures or microvia cracks were seen after drop test.

Conclusion

Stacked microvias PWBs have demonstrated reliability through 2X reflow and rework operations. This evaluation has been conducted as part of qualification work concerning stacked microvia boards for handset assembly. The assemblies survived thermal shock, temperature / humidity and drop shock testing. Since no failures or cracks were seen in the joints or microvias, the assembly passed qualification testing.

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