On the rise. Two such applications are high-speed digital application and modules for hand held devices. For high-speed applications, designing power distribution systems (PDS) is becoming ever more challenging and finding a solution for EMI ever more difficult. The traditional method of coping with these challenges was to use discrete capacitor components by optimising component type, amount and location. However, as LSI technology scales to faster transistors and lower voltage, this traditional method is becoming ineffective, inefficient and costly. Embedded capacitor technology has proven to be effective in overcoming these issues by contributing to providing low impedance PDS and reduced EMI. Here we study the effectiveness of embedded capacitors using commercially available simulation software. The demand for higher HDI meanwhile is endless when it comes to modules for hand held devices. One solution to this demand is to embed capacitor functions inside PWBs. Although various embedded capacitor materials have been proposed, the challenge for PWB fabrication lies in producing uniform and reliable capacitors cost effectively. Here we propose a practical method of forming embedded capacitors and discuss the factors that can affect the tolerance of capacitance value.

**Embedded capacitors for high-speed digital application**

**Power and ground noise simulation**

Two of the major issues facing electrical designers of high-speed digital equipment are PDS and EMI. These phenomena are caused mainly by power/ground resonance noises. Numerous simulation software products supporting electrical designers have been marketed by vendors. We have chosen EMISTREAM developed by NEC to investigate the impact of reducing power/ground resonance by PWB with embedded capacitor. The EMISTREAM simulation is based upon the Spice model and provides an accurate simulation of power and ground resonance noise in a short calculation time of around a few minutes. The parameters required for the ground and power planes are dielectric thickness, dielectric constant and thickness of Copper.

**Simulation results with discrete capacitor components**

The design of the board for simulation was provided by NEC. The board is constructed of 4 layers with the 2nd and 3rd layers used as a power and ground layer. As a default design, 0.6mm FR-4 (Dk=4.6) with 1oz Copper was used as a power and ground layer. 35 decoupling capacitor components (0.1µF) were mounted on the surface to supply power to the LSIs.

Figure 1 shows the power/ground resonance simulated result using the default design. Excitation point (source of noise) was chosen at LSI, indicated as U2 in the figure. The magnitude of noise level is also listed. As can be seen from the figure, there are areas where a significantly high noise area resulted from power and ground resonance (values greater than 0 dB are coloured in red). With the conventional method of placing capacitor components on the surface, it is necessary to decide on the type, amount and location of capacitor components. Figure 2 is the result of placing a minimum amount of capacitor components to reduce the resonance voltage to below 0dB. Although it was possible to achieve 0 dB by adding 44 capacitor components (all 0.1µF), it was necessary to violate the placement location in the circled area of Figure 2. In this circled area, since the LSI is already mounted, it is necessary to mount capacitor components on the backside of the board, which will involve an additional cost for surface mounting.

**Simulation results with embedded capacitor**

Next, we selected a set of embedded capacitor materials, as listed in Table 1, to substitute as a power and ground plane. The embedded
capacitor material has a thickness range of 8 to 24µm and Dk ranging from 4.4 to 30. The embedded capacitance material, Faradflex, is commercially available and used in volume for high-speed digital applications. Details on the properties and processing attributes of the material have been described in previous publications.

Firstly, we conducted a simulation using parameters of BC24, dielectric thickness 24µm, Dk=4.4, the simulated result of which is illustrated in Figure 3. The result showed that power/ground resonance can be reduced dramatically without any additional placement of capacitor components and achieve 0dB noise level. This not only implies that a much lower noise level can be achieved using an embedded capacitor in the power and ground planes, but also that costs may be reduced by eliminating surface mount capacitors. In this case, a total of 44 capacitors were able to be removed from this board, equivalent to 1100 capacitors per square metre.

For certain high-end applications, achieving 0 dB is not enough though, at times the required noise level can be as low as –26 dB. This is due to less margin allowance resulting from the lower operating voltage of LSI. It is generally said that the allowed level of voltage fluctuation is 5%. This is a noise level of –26dB according to the following formula:

\[ dB = 20 \times \log(0.05) = -26 \]

Figure 4a shows the result with the default condition (P/G 0.6mm FR-4, Dk=4.6) with 44 additional capacitor components. The whole board area showed a noise level of over –26dB. In this case, it was impossible to reduce noise level to below –26dB by adding capacitor components. Figures 4b and 4c show the result when BC24 and BC12TM were used as power and ground planes without any additional capacitor components other than 35 default capacitors. With BC24 used in power and ground planes, it was possible to achieve a –26dB noise level. With BC12TM in use, much lower noise levels were achieved. This result implies that with applications that require very low noise levels, the traditional placement of capacitor components becomes obsolete and the role of embedded capacitor technology becomes important.

**Influence of dielectric thickness of embedded capacitor**

In order to understand which property of the embedded capacitor affects the power/ground noise level, a simulation was conducted to determine the impact of the dielectric thickness of embedded capacitor material. As shown in Table 1, the influence of dielectric thickness can be observed by comparing embedded capacitor material with the same Dk value and different thickness – BC24, BC16, BC12 and BC8. In Figure 5, the maximum voltage noise level in each frequency from 1MHz to 1GHz is shown. With 0.6mm FR-4 used in P/G plane, even with additional capacitor component placement, it was difficult to achieve less than –5dB. With an embedded capacitor material used in P/G plane, –26 dB was easily achieved. It was found that the thinner the embedded capacitor material being used, the lower the noise level achieved. For instance, at resonance noise around 550MHz, noise level of PWB using BC24 was around –30dB, BC16 –38dB, BC12 –42dB and BC8 –50dB. This implies that the target noise level can be achieved by selecting embedded capacitance materials of the appropriate thickness.

**Table 1 - Properties of embedded capacitance material**

<table>
<thead>
<tr>
<th>Property</th>
<th>Unit</th>
<th>BC24</th>
<th>BC16</th>
<th>BC12</th>
<th>BC8</th>
<th>BC12TM</th>
<th>BC161</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Thickness</td>
<td>µm</td>
<td>24</td>
<td>16</td>
<td>12</td>
<td>8</td>
<td>6</td>
<td>16</td>
</tr>
<tr>
<td>Cp @1kHz</td>
<td>pF/cm²</td>
<td>190</td>
<td>260</td>
<td>310</td>
<td>500</td>
<td>680</td>
<td>1700</td>
</tr>
<tr>
<td>Dk @1kHz</td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
<td>4.4</td>
</tr>
<tr>
<td>Dl @1kHz</td>
<td>0.019</td>
<td>0.019</td>
<td>0.019</td>
<td>0.019</td>
<td>0.019</td>
<td>0.019</td>
<td>0.019</td>
</tr>
</tbody>
</table>

Figure 4a (left) - 0.6mm FR-4 (Dk=4.6) used as P/G plane; Figure 4b (centre) - BC24 used as P/G plane; Figure 4c (right) - BC12TM used as P/G plane
Influence of dielectric constant of embedded capacitor

Another approach is to use a higher Dk embedded capacitor material on P/G plane. Figure 6 shows the maximum voltage noise in each frequency from 1MHz to 1GHz. There are two sets of comparison shown in this figure. The first set is a comparison between BC12 and BC12TM, in which both materials have a thickness of 12µm but Dks of 4.4 and 10 respectively. In this comparison, not only was the suppression of noise observed with higher Dk material, but also a shift in resonance frequency. The second set of comparison was between BC16 and BC16T, where both materials have a thickness of 16µm but Dks of 4.4 and 30 respectively. In this case too, with high Dk material, the suppression of resonance noise and shift in resonance frequency was once again observed.

The above results suggest that using higher Dk material has the merit of reducing noise level, and that is useful to alternate the resonance frequency to avoid interference with specific frequency of interest without changing the thickness of P/G plane.

RCF type capacitor material and its processing for Module/SiP application

One of the important issues when forming embedded capacitors for module application is the uniformity of capacitance, and we have developed a practical and economical process using RCF type capacitor material. RCF capacitor material is prepared by mixing high Tg epoxy resin with high Dk ceramic nano powder and evenly coating the very low profile Copper foil with the mixed resin. It is supplied in B-stage as standard RCF for HDI applications and is very easy to laminate with core materials and to form a thin high-Dk capacitor layer inside FR-4 multi-layer PWB boards. Though it has a relatively high ceramic content, the high Dk dielectric material shows the insulation resistance, heat resistance and robustness required for standard PWBs. The material is also free from any halogenated substance that may cause environmental hazard, and is available in a thickness range of 8 to 16 µm. No special refrigerated storing conditions are required.

Formation of singulated capacitor with sand blasting process

Although a thin and uniform high Dk dielectric layer is formed inside the PWB by laminating RCF capacitor on the core materials, in order to utilise this layer as singulated capacitors, we need to formulate an appropriate size capacitor to realise the necessary capacitance and then electrically connect the capacitor with other devices, and encapsulate the capacitor to protect from various environments. The removal of unnecessary high Dk dielectric is very important to increase the rate of utilisation of the precious boards area and allow board designers more freedom. Several methods are traditionally utilised to remove unnecessary resin in PWB industry: laser ablation, plasma etching, dissolving by organic solvent and degradation by desmear solution. Several attempts were made using these methods but the conclusion eventually reached was that the sand blasting process (also known as jet scrubbing or wet blasting) is the easiest, most economical and most environmentally friendly process. Sand blasting machines are also very popular in PWB industry for the mechanical surface cleaning process and many board shops are already equipped with sand blasting machines, which can be used in the process of removing high Dk dielectric.

Table 2 - RCF type capacitors from Oak-Mitsui Technologies, MC series

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Condition</th>
<th>Unit</th>
<th>MC16TR</th>
<th>MC12TR</th>
<th>MC8TR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance</td>
<td></td>
<td>pF/mm²</td>
<td>17</td>
<td>22</td>
<td>33</td>
</tr>
<tr>
<td>Dielectric Thickness</td>
<td></td>
<td>µm</td>
<td>0.019</td>
<td>0.019</td>
<td>0.019</td>
</tr>
<tr>
<td>Dielectric Dk</td>
<td></td>
<td></td>
<td>1000</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Peel Strength</td>
<td></td>
<td>kN/m</td>
<td>&gt;0.7</td>
<td>&gt;0.7</td>
<td>&gt;0.7</td>
</tr>
<tr>
<td>Thermal Stress</td>
<td></td>
<td>@ 288°C</td>
<td>&gt;10</td>
<td>&gt;10</td>
<td>&gt;10</td>
</tr>
</tbody>
</table>
thickness of dielectric is substantially stable and unchanged during and after lamination because the flow of RCF capacitor is almost nothing through the lamination process. The upper electrode is formed by the etching process and acts as a resistor while the board is being sand blasted. After sand blasting, lines and vias can be formed by standard HDI process.

As described, the RCF capacitor does not require any special equipment or machinery to process. We therefore believe that this is the easiest, fastest and the most economical way to embed the capacitor inside PCBs and/or packages.

**Capacitance tolerance study of RCF capacitor**

a) Capacitance measurement

When embedding singulated capacitors, one of the most important performances that needs to be achieved is a capacitance tolerance. Applications such as bypass capacitors may allow +/-20%, but applications such as filters may require +/-5%. In order to achieve these tolerances, it is very important to understand how to control the tolerance by embedding capacitors.

A test was conducted to investigate capacitor tolerance formed by using RCF capacitors. Various sizes of capacitors, from 0.0625mm² (250 x 250µm) to 4mm² (2 x 2mm), were formed using the test vehicle shown in Figure 8. Capacitance measurement was conducted using flying probe capacitance measurement equipment from Hioki E.E. The measurement result is shown in Table 3. Regardless of size differences, the variation in tolerance of all capacitors was under 10%.

b) Discussion of capacitance tolerance

The tolerance of capacitance is determined by two main factors. One of the variations of capacitance is due to the non-uniformity of capacitance material itself, the other due to the variation associated with etching variation when forming electrodes for capacitors. The total tolerance of capacitance can be expressed in following equation:

\[
\text{Total tolerance of capacitance} = V1 \text{ (Capacitor material variation, thickness, Dk)} + V2 \text{ (Etching pattern variation)}
\]

V2 can be expressed in functions of D (Target electrode size in mm) and d (Etching variation in µm):

\[
\text{Expected tolerance of capacitance} = V1 \text{ (Variation by dielectric coating)} + V2 \text{ (Etching variation in µm)}:
\]

\[
\text{Expected tolerance of capacitance} = \frac{((D+d)-(D-d)^2)}{D^2/106*100}
\]

With this equation, expected capacitance tolerance can be calculated according to the size of target capacitor electrode and etching variation. Figure 9 shows the simulated results of expected capacitance tolerance in the case of +/-5% capacitance material variation. Each simulate line indicates variation in certain etching variation. For instance in Figure 9, with capability of etching patterns in +/-5µm (circle plot), it is assumed that +/-6% can be achieved when forming 1mm² capacitors and +/-8% can be achieved when forming 0.1mm² size capacitors. In the case of etching capability of +/-15µm (square plot), the expected tolerance would be worse, +/-8% at 1mm² size capacitors and +/-14% at 0.1mm² size capacitors. From these results, not only is the uniformity of capacitance material important in achieving tight tolerance, but also etching capability too, especially in forming small size capacitors.

c) Comparison between simulated result and measurement result

A test was conducted to compare the simulated result and the actual tolerance of capacitors in different capacitor sizes. The capacitor material used in the test was MC16TR with 12micron Cu. Figure 10 shows the actual measured tolerance result from a capacitance size of 0.0625mm² (250 x 250µm) to 4mm² (2 x 2mm). Actual measured capacitance tolerance matched quite well with the simulated result using +/-7µm as an etching variation. This implies that the PCB manufacturer where this test board was fabricated has an etching capability of +/-7µm.
In this case, +/-10% tolerance was achieved with a capacitor size as small as 0.0625mm² (250 x 250µm). Each PCB manufacturer should have different etching capabilities. Once the etching capability of PCB facility is known, it is possible to estimate the expected tolerance of capacitance at each capacitor size using the calculation method described here.

Advantages of embedded capacitance

For high-digital applications, EMIS-stream simulation software showed that the use of embedded capacitance in power and ground plane can be very effective in reducing noise. As LSI speed increases and operation voltage decreases, embedded capacitor PWB technology can offer a cost-effective solution to meet requirements. By using a simulation tool like EMIS-stream, electrical designers can easily understand the advantages of using embedded capacitors in PWBs to reduce power and ground noise and improve power distribution. We hope these simulation tools will accelerate the usage of embedded capacitors for PWBs.

For forming singulated type capacitors, we have demonstrated that an RCF type capacitor material with sand blasting process would be a practical, reliable and economical method. Not only is the uniformity of capacitance material important in forming uniform capacitance, but etching uniformity plays an essential role too, especially when forming small size capacitors.

Ultra-Thin Copper Foils For Ultra Fine Line Formation

Mitsui Mining & Smelting has developed new ultra-thin, 1.5-micron and 3-micron Copper foils for the next generation of High Density Interconnects (HDI). Micro Thin-Ex consists of a special minute nodular treatment that has very low and uniform profile, making it suitable for ultra fine line formation, high frequency boards, and applications where impedance control is critical. The product consists of three layers: the ultra-thin Copper foil, an 18-micron Copper foil carrier to support the ultra-thin Copper foil, and the releasing layer between the two Copper foils. After lamination of the product to a base material, the carrier foil is removed from the laminate.

MicroThin-Ex provides a thin, uniform layer of Copper with excellent peel strength. Once the plating of the features and vias is completed, the extraneous thin Copper can be easily removed in a flash etch process. A Tin coating to protect the features and vias is not required as the flash etching removes minimal material.

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