Smart PWB Manufacturing Technologies

by T. Löher, A. Neumann, B. Pahl, and H. Reichl, Technische Universität Berlin,
A. Ostmann, Fraunhofer Institut für Zuverlässigkeit und Mikrointegration

The inherent functionality of a printed wiring board (PWB) can be dramatically increased by embedding electronic components into the board. For resistors, capacitors and inductors, technological turnkey solutions are offered by major manufacturers and novel technologies are also under development. A further boost of functionality will be accomplished by the integration of active chips into the board. Two approaches for chip integration into the board will be discussed in detail: the chip in polymer (CIP) approach and the embedding of chips into flexible PWBs via a flip chip process.

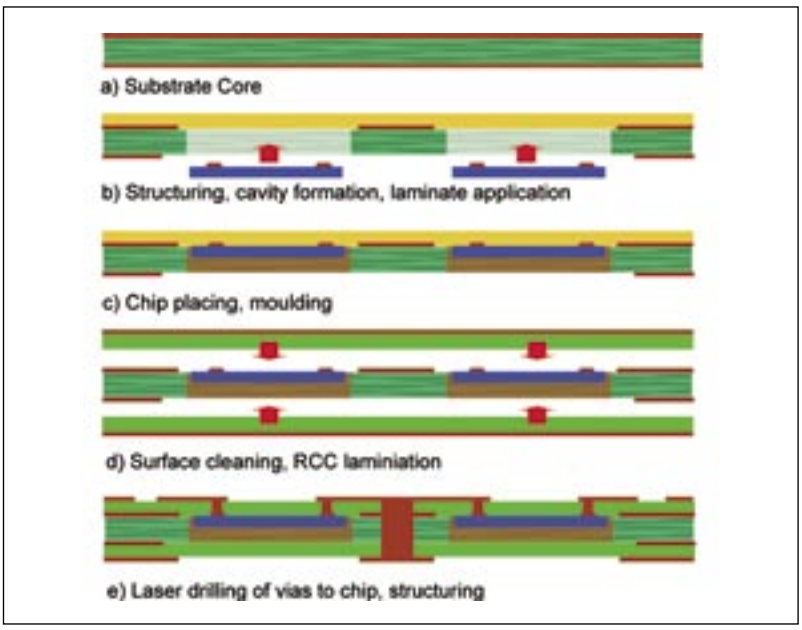


Figure 1 - Integrated Module Board technology process flow

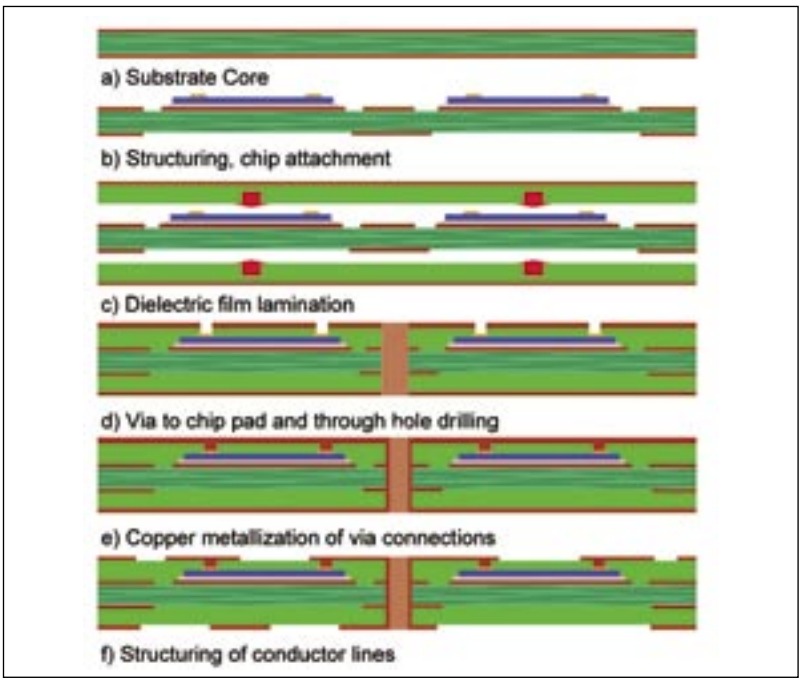


Figure 2 - Chip in polymer schematic process flow

Miniaturisation and functional diversification are the most powerful development drivers in the electronics industry. On the one hand the roadmap appears predetermined by Moore's Law, which refers to semiconductor processing and affects electronic appliances in general. On the other hand diversification manifests itself in the progress and increasing importance of electronics in many application fields where until now it was not the major function. This can be seen, for example, in the increase of electronic instrumentation and control in automotives, the increasing functionality of mobile communication, and human body-adapted medical applications.

The common platforms for electronic assembly are printed circuit boards, either rigid or flexible polymer based materials or ceramics with metal wirings in single or multiple layers. The components and subsystems to be assembled are arranged on the board surface. Depending on the electronic system, the routing of the metal wires within the board has a more or less complex 3-dimensional architecture. For almost four decades efforts have been made to reduce the component count on top of circuit boards and optimise the wiring by embedding passive components into the circuit board. A multitude of technologies for the embedding of passives into circuit boards are now available from different vendors.

The performance density of elec-

tronic systems will experience a further dramatic increase by the embedding of active chips into the circuit board, the board itself thereby becoming the package of a more complex subsystem.

Passive component embedding technologies

Since rather large ranges of values with tight tolerance for resistors and capacitors are required for most applications, different technologies and issues have to be mastered for the embedding of passive components.

Embedded capacitors

The process technology for embedding capacitors is more or less the same for most commercially available products: capacitor sheets are purchased from the supplier, structured on one side, laminated onto the substrate, and subsequently structured on the other side to form the counter electrode. Although the process technology is similar, due to the different materials and technologies used to apply the dielectric, there is a wide variation in sheet capacitance values. Dielectrics are classified into paraelectrics (low ε_r) and ferroelectrics (high ε_r). Although the former generally result in low sheet capacitance values, the electrical performance of paraelectrics is better due to their higher stability under temperature changes and reduced sensitivity to frequency and bias voltage (generally decreasing with applied frequencies and voltages). The use of embedded capacitors, especially for the power distribution system in the periphery of an active device, offers many advantages over conventional surface mount devices.

Embedded resistors

• Stencil or screen-printing of resistive pastes (generally carbon particle filled polymers). Large resistor value ranges can be covered with appropriately adapted paste compositions. Variations in printed

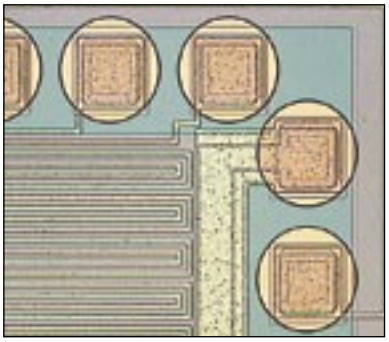


Figure 3 - Sputtered TiW/Cu layer over Al bondpads

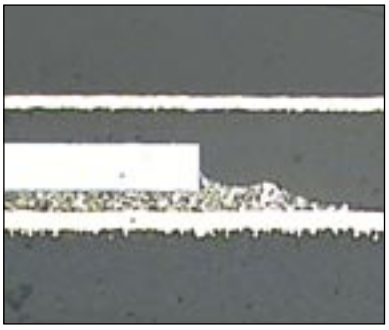


Figure 4 - Embedded chip in a RCC layer

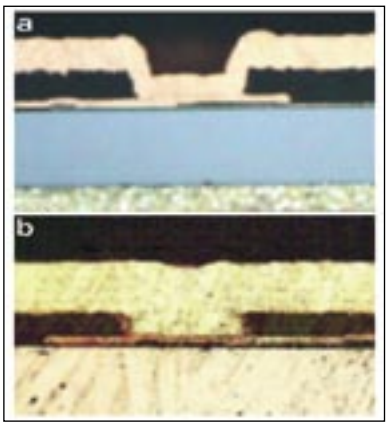


Figure 5 - Microvias to embedded chips metallized with electroless plating and (a) DC electroplating (b) reverse pulse plating

resistor values, however, are much too large for most applications and printing is therefore generally followed by the laser trimming of the resistors. The effect of subsequent lamination into an inner layer of the board is yet another issue that impedes the straightforward use of this technology.

• Thin film technologies are available that allow resistors to be fabricated with a smaller value spread evenly, without additional trimming, e.g. ± 4%. Application of the resistor structures onto the board can be achieved by the lamination of Copper sheets that are coated with a thin film resistor layer (Ni or Pt resistor layers) followed by a two-step structuring/etching process, or additive plating (electroless Ni(P)) onto pre-structured substrates. One drawback of this technology is that sheet resistances are today limited to values between 250 (Ni) and 1000 (Pt) Ohm/square. Reasonable resistor values are therefore limited to values below 10 kOhm. Another problem is that power dissipation capabilities generally decrease with increasing sheet resistance.

Embedded inductors

No additional technology is necessary for the embedding of inductors. Spiral or rectangular inductors can be patterned directly on a metal layer on the circuit board. However, the electrical properties have to be simulated and tested in detail for any given combination of metal wire geometries and embedding materials.

Embedding of active devices

Three alternative technologies for chip embedding are presented here. Each one lays great emphasis on exploiting as far as possible the base technologies currently used by printed circuit board manufacturers.

Integrated module board technology

Integrated module board (IMB) technology was developed at Helsinki University in the late 90's. Starting with a conventional rigid substrate core material, after the structuring of the metal layers, a cavity with lateral dimensions similar to that of the chip is made through the core to take in the chip. A laminate layer to take up the chip is then applied to the board, whereupon the chip is aligned and placed in the cavity using a high accuracy flip chip bonder. The alignment inside the core is bet-

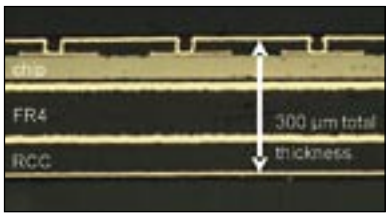


Figure 6 - Chip embedded in a substrate with thin core (via metallization only by electroless Cu)

ter than +/- 5 µm. The cavities are then filled with a molding polymer that is chemically, mechanically and electrically compatible with the chip, the substrate, and the build up materials. After the curing of the thermosetting epoxy, the laminate is removed and the board is cleaned of residues and impurities. The core is then laminated on both sides with a resin coated Copper (RCC) foil and microvias to the chips are fabricated. The outer layers are manufactured by semi-additive pattern plating and etching. Finally a solder mask is applied and the pads for the components are coated with an organic surface protection or a thin gold layer.

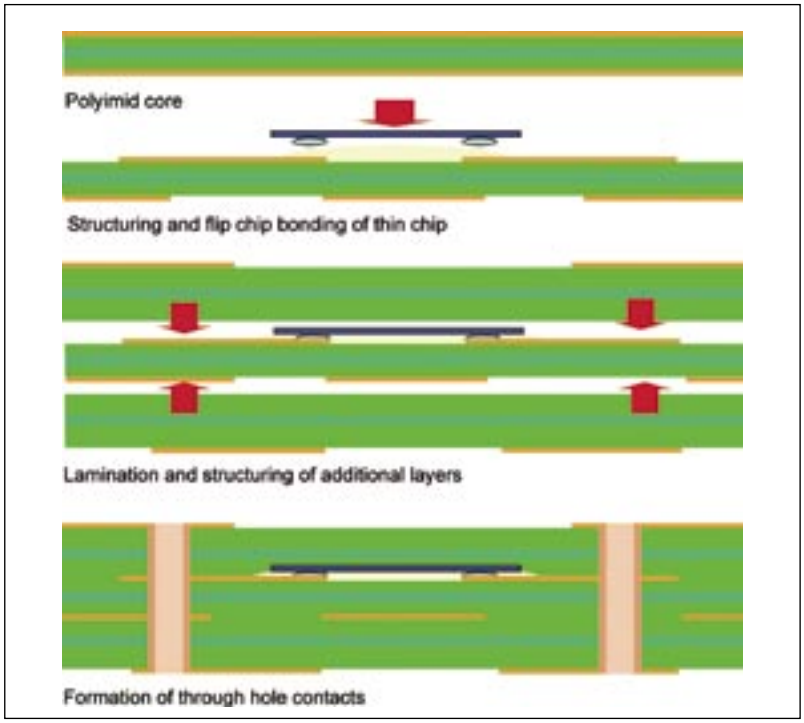
With IMB technology it is possible to embed components with a range of thicknesses. However, wire board manufacturers are generally reluctant to have a cavity in the core layer of the board as this can bring undesired fragility with it.

Chip in polymer

The technology developed at TU Berlin works without a cavity layer in the wire board. Very thin chips are placed directly on top of the core substrate. Chips thinned down to 50 µm are placed and attached onto the board with great precision using an adhesive or die attach film. The chip is then embedded in a polymer layer by vacuum lamination. Vias to the chip contact pads and to the Cu-routing on the board are formed by laser drilling and metallization, and finally the top Cu-layer is structured. The structure now allows conventional components to be positioned directly over the embedded chip.

The process technology is currently under development for large-scale production capabilities and is supported by the European Union in the Hiding Dies project. The CIP process comprises various phases: wafer and chip preparation; the die bond process; chip lamination; via drilling; Cu interconnect.

Figure 7 - Schematic process flow of the embedding of thin chips into a flexible wiring board



Wafer and chip preparation

Conditioning of the chips for the embedding process is achieved most cost effectively in wafer level processes. First the Al or Cu contact pads of semi-conductor chips are reinforced in order to be compatible with the laser drilling process. Thinning of the wafers to 50 µm is usually performed by a subcontractor.

For dicing, wafers are mounted onto a UV dicing tape. A careful selection of dicing blades and parameters is necessary. After dicing, the tape is exposed to UV light.

The die bond process

The challenge of thin die bonding is to achieve a low bond-line thickness. Embedding into a build-up layer limits the allowed thickness of chip and die bond adhesive. Together it should be less than the dielectric thickness, leaving about 15-20 µm of dielectric over the chip after embedding. If not, planar embedding is impossible and the chip might be damaged. Screen-printing allows for closer control over the volume and location of the adhesive paste, which is more difficult to manage by dispensing. Using an electrically conductive Ag-filled paste enabled a bondline thickness of 16 µm to be achieved.

An alternative is the use of b-stage paste. After printing it is dried and becomes non-tacky. It allows for the decoupling of printing and die attach. After drying, boards can be stored or moved to other locations. During die bonding the boards or chips have to be heated in order to achieve a surface tackiness again. Chips bonded with b-stage adhesive have shown less voids compared to standard material.

Die attach film can also be used for the same purpose. This is a UV dicing tape with two layers: a conventional UV dicing foil and an adhesive layer on top. Wafers are mounted to this adhesive layer. The dicing blade has to cut the silicon and the top layer of the tape. In the picking process this layer remains at the chip and

serves as adhesive. In order to tack the chips to the substrate, it has to be heated.

This chip embedding technology needs a fast and accurate die bonder that is capable of handling 50 µm thin dies and which provides adjustable temperature for the bond head and the substrate chuck. Accuracy also plays a crucial role. The tolerances of the sequence die bonding, via drilling and Cu structuring have to be very low in order to achieve an acceptable yield. One requirement is that the machines for these three process steps use the same fiducials on the core for alignment.

Chip lamination

The chips are effectively embedded into the PCB structure by vacuum lamination and the core substrate with the die-bonded chips is covered from both sides with a RCC layer. A press book consisting of separation films, pressure distribution material and steel plates is used. The vacuum in the press chamber ensures the void-free distribution of the RCC dielectric.

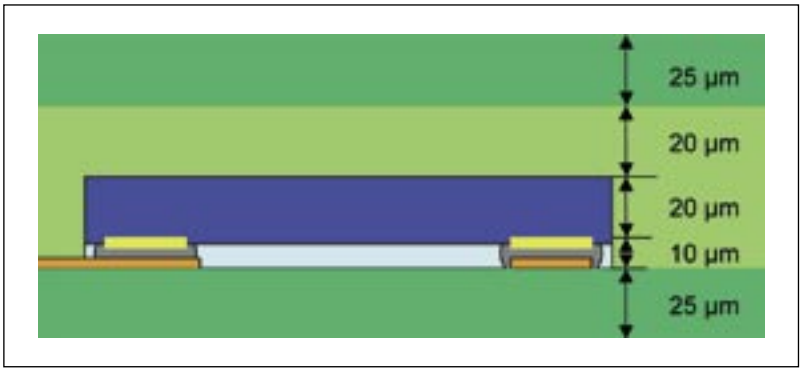


Figure 8 - Representation of a thin chip in the flexible wiring board

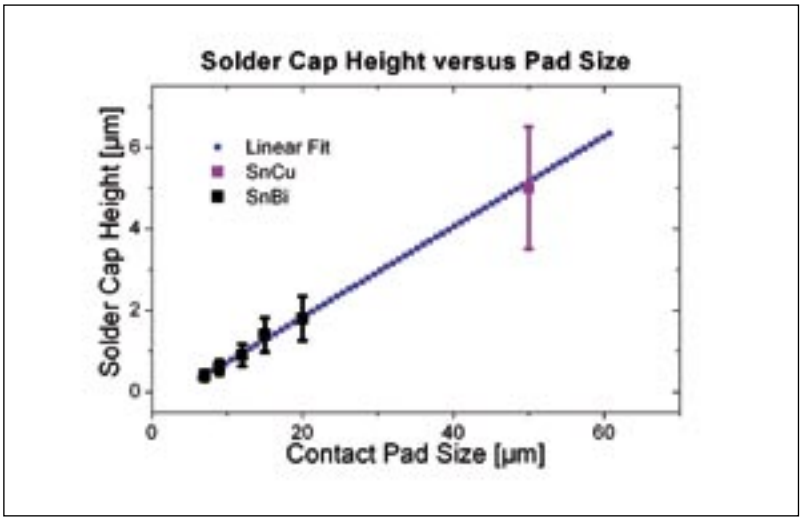


Figure 9 - Thickness of a solder cap after immersion into the liquid solder a function of the contact pad size

The lamination profile is a compromise between low pressure to protect the chips, and high pressure for flow and curing. A high flow, high Tg RCC is used to obtain optimum results. The kiss pressure needs to remain low to prevent from introducing cracks in the silicon; however, a minimum level is required to sustain sufficient flow around the chips. The used RCC requires 40 min curing at a temperature above 175°C. To minimise warpage, at the end of the cycle the boards are cooled under pressure.

One important parameter is the resulting epoxy thickness on top of the embedded die, after lamination. This thickness will determine the possibility of making small microvias for contacting the I/O pads of the chip. The uniformity of the covering epoxy layer is important for the process window of the laser drilling. A 15 – 20 µm epoxy layer on top of the embedded die, as shown in Figure 4, is considered a good compromise between the laser drilling margin and the ability to create small microvias.

Via drilling

The current method of handling contact pitches of 150 µm is by forming vias directly to the chip pads. The laser drilling of vias to the bond pads of embedded chips is comparable to the established formation of microvias on PCBs. Holes are opened in the Cu layer of the RCC over the contact pads and the dielectric then removed by a laser until the Cu bump is reached. The walls of the vias are then metallized as described in the following section. Tight positioning tolerances and small via sizes represent the major challenges here. A pulsed 355 nm UV laser is used for the drilling process at TU Berlin.

In a production environment, using a dual beam machine, firstly the top Cu layer is opened by a 355 nm UV laser, cutting only slightly into the dielectric. Then a fast ablating CO2 beam drills down to the bump, without etching the Cu. The cost of equipment is relatively high but this method allows the fastest drilling with speeds up to 150 holes/s.

Cu interconnect

After laser drilling, the microvias are cleaned in a desmear step (KMnO4 @ 65°C). This is followed by Pd activation and electroless Cu deposition. The Cu layer is 1 – 2 µm thick and acts as a seed layer for the subsequent galvanic plating. A minimum thickness of 10 µm Cu is required in the microvias (Figure 5a). Some experiments have been done with reverse pulse plating in order to completely fill the microvias with Cu (Figure 5b).

Daisy chain electrical measurements containing microvias to the chip and microvias to the core substrate have been made and show

good uniformity of the contacts. A good example can be seen in Figure 6, which displays a cross-section of a module with 100 µm core. The total thickness of this very thin device is only 300 µm.

Chip embedding into flex

The embedding of chips into flexible wiring boards can increase the functional density of electronic systems even more than the above-described technologies. The benefits of flex substrates, such as their lightness and high wiring density, will here be joined with the complexity of the active chip. However, in order to maintain the basic flex substrate characteristics, build-up with an integrated chip has to be as small as possible. Chips with a thickness of only 20 µm are used and the interconnection thickness should not exceed a couple of microns.

The technology under development at TU Berlin comprises the flip chip type mounting of the thin chip onto the flex substrate and the lamination of the structure on both sides. Contacts to outer layers are made with through holes (see Figure 7). Further layers can be processed on the build up. Process technologies for the embedding of passive and active components into flex wiring boards are developed and investigated by the European Union-funded project, Shift.

Figure 10 - Ultra thin contact with a Cu wiring on the bottom a thin layer of solder/ intermetallic and a top Ni contact

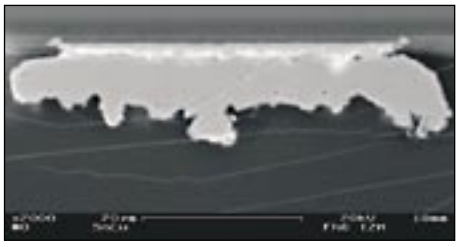


Figure 11 - Thin chip laminated with epoxy resin coated cover lay

Wafer preparation

First the bond pads of the chips are equipped with a solderable under bump metallization then Ni(P) is deposited in an electroless process onto the otherwise unsolderable Al pads of the chips. The Ni bump height is between 3 and 5 µm (± 3 %). SnCu solder is deposited onto the Ni bump by an immersion soldering process. Small solder caps are formed on the Ni when the wafer is pulled out of the liquid solder at a temperature of 270°C. The average heights of the bumps depend on the size of the Ni pad (which is 40 µm for the test vehicle under investigation at TU Berlin - see Figure 9). However, the variation in bump height for a given pad size is very large: ± 50 %. This variation is levelled out in the subsequent thermode bonding processes, where an excess of solder is squeezed to the side of the interconnection. Intermetallic phases form at the interface between solder and Ni but enough solder remains to allow for a subsequent bonding process.

Wafer thinning

The thinning process takes place alongside the dicing of the single chips. First the chips on the wafer are separated either by sawing or by etching. The etching or sawing lines go 25 to 30 µm deep into the wafer.

After die separation the wafer is attached to a UV-release grinding tape. The wafer is ground to a thickness of 50 to 60 µm in the first step at high speed (300 µm/min) then spin etched at a rate of 30 – 40 µm/min to the final thickness of 20 µm.

Proper release of the chips from the tape is crucial for further processing. The solder caps in particular have to be free of contamination in order to remain solderable to the flex substrate Cu wiring. UV release tape turned out to be most suitable in this respect.

Thermode bonding to the flex substrate

Single chips are subsequently thermode bonded to the Cu-wiring of the flex substrate. The flex polyimid (PI) is fabricated using photolithography and the etching of the Cu on the PI. Thermode bonding is performed with commercial flip chip assembly equipment. The use of no flow underfill is mandatory to warrant the integrity chip interconnection to the substrate and to make sure that no voids or air bubbles remain under the chip. One challenge is to dispense a suitable volume of underfill: too much and there is an undesired flow of underfiller onto the topside of the chip, too little won't fill the gap between chip and substrate. This problem can be resolved with screen-printing.

The pressure and temperature profiles of the bonder are adapted to the melting temperature of the solder bumps, ~230°C, and the curing characteristics of the no flow underfiller.

Lamination

Even though the chips are thin, lamination has to be performed without damaging the test vehicle chip. For the different adhesive systems, the lamination parameters were 30 kg/cm^2 with 190°C for 3 minutes (epoxy resin, see Figure 11) and 180°C with 20 kg/cm^2 for 2 hours respectively (acrylic based glue).

Contacting

Since the chips are flip chip bonded onto the flex substrate with a structured Cu wiring, contacting to other layers of the build up can be accomplished either by conventional through hole technique or by blind vias drilled with a laser.